XL710
REFERENCE SCHEMATICS

REV 1.0
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REVISION HISTORY

0.1  -- INITIAL DRAFT

0.5  -- RELEASE VERSION

0.75 -- UPDATED SERIES RESISTORS FOR SMBUS, SERIES RESISTORS TO NC-SI RX
       ADDED JTAG HEADER, AND VOLTAGE LEVEL LABELS.
       REMOVED BACKUP MARGINING CONNECTION.

1.0  -- ADDED JUMPER TO ENABLE DEBUG MODE
       ADDED LED SETTING DESCRIPTIONS
       REMOVED REFERENCE TO CFGID THAT ARE NOT SUPPORTED
FUNCTIONAL BLOCK DIAGRAM

XL710
4x 10Gbe
2x 40Gbe
ETHERNET CONTROLLER

PORT 0
LED I2C SDP
SFP+ OR QSFP+

PORT 1
LED I2C SDP
SFP+ OR QSFP+

PORT 2
LED I2C SDP
SFP+

PORT 3
LED I2C SDP
SFP+

HOST
PCIE GEN3 X8
SMBUS

25 MHz
XTAL CIRCUIT
25 MHz
LVPECL OR CML
DIFF OHC

OPTIONS:
BACKPLANE
SFP+ OR QSFP+

FLASH

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NETWORK DIVISION
2111 N.E. 25TH AVENUE
HILLSBORO, OR 97124

TITLE
XL710 REFERENCE SCHEMATICS

SIZE
B

CODE

DOCUMENT NUMBER

REV
1.0

DATE
06/18/2013

SHEET
4
XL710 (PAGE 1 OF 6)

ROUTE AS 85 OHM DIFFERENTIAL PAIRS.
TRADES WITHIN A PAIR MUST BE MATCHED
WITHIN 1 INCH. PAIRS TO PAIRS TRACES LENGTHS SHOULD BE MATCHED WITHIN 1 INCH.
FOR MORE GUIDELINES SEE DATASHEET.

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PLACE CAPACITORS WITHIN 5 MILS. PAIR TO PAIR TRACES SHOULD BE MATCHED WITHIN 1 INCH.

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PLACE CAPACITORS WITHIN 5 MILS. PAIR TO PAIR TRACES SHOULD BE MATCHED WITHIN 1 INCH.

PLACE CLOSE TO CONTROLLER. TOTAL TRACE LENGTHS SHOULD BE < 1 INCH.
XL710

(PAGE 6 OF 6)

STRAP HIGH TO ENABLE DEBUG MODE
STRAP LOW FOR NORMAL OPERATION

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LEDS
2X40GBE
CFGID 4.5

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</tbody>
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VCCD REGULATOR EXAMPLE 1: LTC3833