



MegaCore IP Library

Release Notes and Errata



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These release notes cover versions 10.0 through 11.0 of the Altera® MegaCore® IP Library. The chapters in these release notes describe the revision history and errata for each product in the MegaCore IP Library.



From v8.0 onwards, this document replaces all individual IP product release notes and errata sheets that Altera previously published.

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

The product errata tables use the following indicators:

- A checkmark “✓” indicates an issue is applicable to that version
- “Fixed” indicates the issue was fixed in that version
- A dash “—” indicates the issue is not applicable to that version



For the most up-to-date errata for this release, refer to the latest version of the *MegaCore IP Library Release Notes* on the Altera website.



For more information about Quartus® II issues, refer to the *Quartus II Software Release Notes*.

Trademarks

These release notes use the following Altera trademarks:

- Arria® devices
- Avalon® interface
- Cyclone® devices
- HardCopy® devices
- MegaCore function
- MegaWizard™ Plug-In
- ModelSim® simulator
- Nios® II processor
- Quartus II software
- SignalTap® II logic analyzer
- Stratix® devices

System Requirements

The MegaCore IP Library is distributed with the Quartus II software and downloadable from the Altera website, www.altera.com.



For system requirements and installation instructions, refer to *Altera Software Installation and Licensing*.

Revision Dates

The chapters in this document, MegaCore IP Library Release Notes and Errata, were revised on the following dates.

- | | |
|-------------|--|
| Chapter 1. | 8B10B Encoder/Decoder |
| | Revised: 15 May 2011 |
| Chapter 2. | 10GBASE-R PHY |
| | Revised: 15 May 2011 |
| Chapter 3. | 10-Gbps Ethernet MAC |
| | Revised: 1 July 2011 |
| Chapter 4. | ASI |
| | Revised: 15 May 2011 |
| Chapter 5. | CIC |
| | Revised: 15 May 2011 |
| Chapter 6. | CPRI |
| | Revised: 15 May 2011 |
| Chapter 7. | CRC Compiler |
| | Revised: 15 May 2011 |
| Chapter 8. | DDR and DDR2 SDRAM Controller Compiler |
| | Revised: 15 May 2011 |
| Chapter 9. | DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP |
| | Revised: 15 July 2011 |
| Chapter 10. | DDR2 and DDR3 SDRAM Controller with UniPHY |
| | Revised: 15 July 2011 |
| Chapter 11. | DDR3 SDRAM Controller with ALTMEMPHY IP |
| | Revised: 15 July 2011 |
| Chapter 12. | FFT |
| | Revised: 1 July 2011 |
| Chapter 13. | FIR Compiler |
| | Revised: 15 May 2011 |
| Chapter 14. | FIR Compiler II |

	Revised:	15 May 2011
Chapter 15.	Interlaken	
	Revised:	15 May 2011
Chapter 16.	Interlaken PHY	
	Revised:	15 May 2011
Chapter 17.	IP Compiler for PCI Express	
	Revised:	15 July 2011
Chapter 18.	NCO	
	Revised:	15 May 2011
Chapter 19.	Nios II Processor	
	Revised:	15 May 2011
Chapter 20.	PCI Compiler	
	Revised:	15 May 2011
Chapter 21.	POS-PHY Level 4	
	Revised:	15 May 2011
Chapter 22.	QDR II SRAM	
	Revised:	15 May 2011
Chapter 23.	QDR II and QDR II+ SRAM Controller with UniPHY	
	Revised:	15 July 2011
Chapter 24.	RapidIO	
	Revised:	15 July 2011
Chapter 25.	Reed-Solomon Compiler	
	Revised:	15 May 2011
Chapter 26.	Reed-Solomon II	
	Revised:	15 May 2011
Chapter 27.	RLDRAM II	
	Revised:	15 May 2011
Chapter 28.	RLDRAM II Controller with UniPHY	
	Revised:	15 July 2011
Chapter 29.	SDI	
	Revised:	1 July 2011
Chapter 30.	SerialLite II	
	Revised:	15 May 2011
Chapter 31.	Stratix V Hard IP for PCI Express	
	Revised:	15 July 2011
Chapter 32.	Triple Speed Ethernet	

Revised: *1 July 2011*

Chapter 33. Video and Image Processing Suite
Revised: *1 July 2011*

Chapter 34. Viterbi Compiler
Revised: *15 May 2011*

Chapter 35. XAUI PHY
Revised: *15 May 2011*

Revision History

Table 1–1 shows the revision history for the 8B10B Encoder/Decoder MegaCore function.



For more information about the new features, refer to the *8B10B Encoder/Decoder MegaCore Function User Guide*.

Table 1–1. 8B10B Encoder/Decoder MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	Final support for Arria II GX, Stratix IV GX, Cyclone III LS, Cyclone IV GX, and Cyclone IV E devices.
10.1	December 2010	Final support for Stratix IV GT devices.
10.0	July 2010	Maintenance release.

Errata

No known issues in v11.0, v10.1, and v10.0.

Revision History

Table 2–1 shows the revision history for the 10GBASE-R PHY IP core.



For more information about the new features, refer to the “10GBASE-R PHY IP Core” chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 2–1. 10GBASE-R PHY Revision History

Version	Date	Description
11.0	May 2011	Quartus II 11.0 release.
10.1	December 2010	Added Stratix V support.
10.0 SP1	September 2010	Added simulation support.
10.0	July 2010	First release.

Errata

Table 2–2 shows the issues that affect the 10GBASE-R PHY IP core versions 11.0, 10.1, and 10.0.

Table 2–2. 10GBASE-R PHY Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	rx_oc_busy Port Is Not A Top-Level Signal	✓	—	—
	FIFO Full Signals Are Swapped	Fixed	✓	✓
	rx_ready Bit Does not Update When Synchronization Is Lost	Fixed	✓	✓
15 Dec 10	Incorrect Device Support Listed 10GBASE-R PHY IP Core User Guide	—	Fixed	✓
15 Dec 10	Mixed Language Simulation Fails when Optimization Is On	✓	✓	—

rx_oc_busy Port Is Not A Top-Level Signal

The *10GBase-R PHY IP Core* chapter of the *Altera Transceiver PHY IP Core User Guide* describes the rx_oc_busy signal as a top-level signal of the IP core; however, this signal is now included in the reconfiguration bus.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue will be fixed in a future version of the *Altera Transceiver PHY IP Core User Guide*.

FIFO Full Signals Are Swapped

The TX_FIFO_FULL and RX_FIFO_FULL status bits are swapped.

Affected Configurations

This issue affects Stratix IV and Stratix V implementations of the 10GBASE-R PHY.

Workaround

The workaround is to note that for the 10.1 release RX_FIFO_FULL is actually stored as bit 3 of address 0x82 and TX_FIFO_FULL is stored as bit 4 of address 0x82.

Solution Status

This issue will be fixed in a future version of the 10GBASE-R PHY IP core.

rx_ready Bit Does not Update When Synchronization Is Lost

The RX_DATA_READY which is bit 7 of the PCS status register (0x82) does not deassert when synchronization is lost.

Affected Configurations

This issue affects both Stratix IV and Stratix V implementations of the 10GBASE-R PHY.

Workaround

The workaround is to monitor the internal signals that indicate lock status and perform a digital reset of the channel when synchronization is lost.

Solution Status

This issue will be fixed in a future version of the 10GBASE-R PHY IP core.

Incorrect Device Support Listed 10GBASE-R PHY IP Core User Guide

The *10GBase-R PHY IP Core* chapter of the *Altera Transceiver PHY IP Core User Guide* states that the 10GBASE-R IP Core provides final support for the Stratix IV E device family; however, the 10GBASE-R PHY IP core provides no support for Stratix IV E devices.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 10.1 of the *Altera Transceiver PHY IP Core User Guide*.

Mixed Language Simulation Fails when Optimization Is On

Simulation fails when using ModelSim with mixed-languages.

Affected Configurations

This issue affects mixed language simulation including Verilog modules and VHDL entities when optimization is on.

Workaround

The workaround is to turn ModelSim optimization off by using the `-novpt` option to the `vsim` command.

Solution Status

This issue may be fixed in a future version of ModelSim.

Revision History

Table 3–1 shows the revision history for the 10-Gbps Ethernet (10GbE) MAC MegaCore function.



For more information about the new features, refer to the *10-Gbps Ethernet MAC MegaCore Function User Guide*.

Table 3–1. 10-Gbps Ethernet MAC MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Cyclone IV GX, Arria II GZ and HardCopy IV GX devices. Added preamble passthrough mode, datapath option, and PFC features.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ and Stratix V devices. Final support for Arria II GX and Stratix IV devices.
10.0	July 2010	Initial release.

Errata

Table 3–2 shows the issues that affect the 10-Gbps Ethernet MAC MegaCore function v11.0, v10.1 and v10.0.

Table 3–2. 10-Gbps Ethernet MAC MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
1 Jul 11	Data Transmission Not Resumed Immediately When 10GbE MAC Receives PFC Frame	✓	—	—
	Error When Generating Simulation Model Using MegaWizard Plug-in Manager	✓	—	—
15 May 11	Recovery Failure for 10GbE MAC with 10GBASE-R PHY Design Example in Stratix IV Devices	✓	—	—
	TimeQuest Timing Analyzer Failure for 10GbE MAC with 10GBASE-R PHY Design Example in Stratix V Devices	✓	—	—
	64-bit ModelSim Simulator Fails to Simulate 10GbE MAC with XAUI PHY Design Example	✓	—	—
15 Jul 10	No Length Checking for VLAN and Stacked VLAN Frames	Fixed	✓	✓
15 July10	Simulation Not Supported for Stratix V Designs	✓	✓	✓

Data Transmission Not Resumed Immediately When 10GbE MAC Receives PFC Frame

When the 10GbE MAC receives a PFC frame with the instruction to resume data transmission on priority queue n , the MAC does not deassert the `avalon_st_rx_pfc_pause_data[n]` signal immediately and the data transmission on priority queue n does not resume immediately.

Affected Configuration

This issue affects all 10GbE MAC designs with the PFC enabled.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

Error When Generating Simulation Model Using MegaWizard Plug-in Manager

When you use MegaWizard Plug-in Manager to generate a simulation model for the IP core, you may get an error message if the Quartus II software installation directory has empty spaces in the directory path. The Quartus II software displays a warning message similar to the following:

```
Error: add_fileset_file: No such file <Quartus II installation directory path>/ip/altera/ethernet/altera_eth_10g_mac/list_of_files.tcl while
executing "add_fileset_file list_of_files.tcl OTHER PATH
list_of_files.tcl" (procedure "testbench_proc" line 2) invoked from within
"testbench_proc dd"
```

Affected Configuration

All configurations.

Workaround

To avoid this issue, do not type empty spaces in the directory name when you specify the installation directory for the Quartus II software.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

Recovery Failure for 10GbE MAC with 10GBASE-R PHY Design Example in Stratix IV Devices

When you compile the 10GbE MAC with 10GBASE-R PHY design example in Stratix IV devices, the Quartus II TimeQuest Timing Analyzer reports a failure in the Recovery timing analysis report.

Affected Configuration

This issue affects the 10GbE MAC with 10GBASE-R PHY design example in Stratix IV devices.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

TimeQuest Timing Analyzer Failure for 10GbE MAC with 10GBASE-R PHY Design Example in Stratix V Devices

When you compile the 10GbE MAC with 10GBASE-R PHY design example in Stratix V devices, the Quartus II TimeQuest Timing Analyzer reports a failure in the Clock Setup timing analysis report. It may also report a failure in the Clock Hold timing analysis report.

Affected Configuration

This issue affects the 10GbE MAC with 10GBASE-R PHY design example in Stratix V devices.

Workaround

To avoid this issue, follow these steps before compiling the design example:

1. Open the SDC constraint file **top.sdc** in the **altera_eth_10g_mac_base_r** directory.
2. Add the following line to the file:

```
set_clock_groups -exclusive -group {clk_50Mhz} -group  
{*|ch[0].sv_xcvr_10gbaser_native_inst|tx_pll|altera_pll_156M~PLL_OUTPUT  
_COUNTER|divclk}
```

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

64-bit ModelSim Simulator Fails to Simulate 10GbE MAC with XAUI PHY Design Example

When you simulate the 10GbE MAC with XAUI PHY design example in the 64-bit ModelSim simulation software, the simulation fails. The design example contains the JTAG to Avalon Master Bridge core which does not support the 64-bit ModelSim simulation software.

Affected Configuration

This issue affects the 10GbE MAC with XAUI PHY design example that contains the JTAG to Avalon Master Bridge core.

Workaround

Run the ModelSim simulation software in 32-bit mode to simulate the 10GbE MAC with XAUI PHY design example.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

No Length Checking for VLAN and Stacked VLAN Frames

The IP core does not perform length checking on all VLAN and stacked VLAN frames.

Affected Configuration

All configurations.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the 10-Gbps Ethernet MAC MegaCore function.

Simulation Not Supported for Stratix V Designs

The IP core does not support simulation for designs that target Stratix V devices.

Affected Configuration

All configurations.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

Revision History

Table 4–1 shows the revision history for the ASI MegaCore function.



For more information about the new features, refer to the *ASI MegaCore Function User Guide*.

Table 4–1. ASI MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	Final support for Arria II GZ, Cyclone III LS, and Cyclone IV GX devices.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Arria II GX devices.
10.0	July 2010	Maintenance release.

Errata

Table 4–2 shows the issues that affect the ASI MegaCore function v11.0, 10.1, and 10.0.



Not all issues affect all versions of the ASI MegaCore function.

Table 4–2. ASI MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	The Quartus II Software Indicates Support for Arria II GX as Preliminary	✓	—	—
15 Feb 11	ASI Does Not Support VHDL Functional Simulation Model for Cyclone IV GX	✓	✓	—
15 Dec 10	ASI 10.1 Does Not Support Qsys	✓	✓	—
01 Dec 06	NativeLink Does Not Support Gate-Level Simulation	✓	✓	✓

The Quartus II Software Indicates Support for Arria II GX as Preliminary

The Quartus II software version 11.0 issues an incorrect warning indicating that the support for Arria II GX devices is preliminary. The Arria II GX support for the ASI MegaCore function is final.

Affected Configurations

This issue affects all configurations.

Design Impact

None.

Workaround

Ignore the warning.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

ASI Does Not Support VHDL Functional Simulation Model for Cyclone IV GX

Serial loopback designs that target Cyclone IV GX devices using the VHDL functional simulation model fail to simulate.

Affected Configurations

This issue only affects designs that target Cyclone IV GX devices using the VHDL functional simulation model.

Design Impact

The design fails to simulate using the VHDL functional simulation model.

Workaround

Use the Verilog HDL functional simulation model instead.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

ASI 10.1 Does Not Support Qsys

You will not be able to generate the ASI MegaCore function v10.1 using Qsys. Adding the ASI MegaCore function in a Qsys system triggers the following warning message:
ASI does not support Qsys-compatible generation

Affected Configurations

This issue affects all configurations.

Design Impact

The design will not generate successfully in Qsys.

Workaround

Use SOPC Builder instead.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

NativeLink Does Not Support Gate-Level Simulation

When using the NativeLink simulation example, the gate-level simulation design fails.

Affected Configurations

This issue affects all simulators supported by NativeLink.

Design Impact

This issue only affects simulation and does not affect the design compilation.

Workaround

Perform an RTL simulation of the NativeLink simulation example.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

Revision History

Table 5–1 shows the revision history for the CIC MegaCore function.


 For information about the new features, refer to the *CIC MegaCore Function User Guide*.

Table 5–1. CIC MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.

Errata

Table 5–2 shows the issues that affect the CIC MegaCore function v11.0, v10.1, and v10.0.

Table 5–2. CIC MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices	✓	—	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—

Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices

The CIC MegaCore function v11.0 provides final support for Arria II GZ and Cyclone IV GX devices. However, when your CIC MegaCore function targets an Arria II GZ device or a Cyclone IV GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All CIC MegaCore function variations that target an Arria II GZ device or a Cyclone IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the CIC MegaCore function.

Compilation Targeting a Stratix V Device Fails

Designs that include a CIC IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

CIC IP core designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Revision History

Table 6–1 shows the revision history for the CPRI MegaCore function.



For information about the new features, refer to the *CPRI MegaCore Function User Guide*.

Table 6–1. CPRI MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Upgraded to final support for Arria II GZ and Cyclone IV GX devices. Upgraded to HardCopy Compilation support for HardCopy IV GX devices. Added byte-enable signal. Added parameter to control WIDTH_RX_BUF.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> Added support for Arria II GZ devices. Added support for additional CPRI data rates in Arria II GX devices. Added scrambler/descrambler support. Added CPU interrupt for remote hardware reset.
10.0	July 2010	<ul style="list-style-type: none"> Added support for Cyclone IV GX devices. Added GUI parameter to enable auto-rate negotiation and two signals to support visibility of the feature status. Enhanced testbench suite to include two new testbenches, to demonstrate operation with no MAP interface and to demonstrate auto-rate negotiation.

Errata

Table 6–2 shows the issues that affect the CPRI MegaCore function v11.0, v10.1 SP1, v10.1, and v10.0.



Not all issues affect all versions of the CPRI MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

Table 6–2. CPRI MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		11.0	10.1 SP1	10.1	10.0
15 May 11	Hold Time Failures at Line Rate 2457.6 Mbps on Arria II GX Devices	✓	—	—	—
	Cannot Simulate Auto-Rate Negotiation in VHDL Models that Target Arria II GZ, Cyclone IV GX, and Stratix IV GX Devices	✓	—	—	—
	CPRI_ROUND_DELAY Register Value is Wrong by Eight Clock Cycles	Fixed	✓	✓	✓

Table 6–2. CPRI MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		11.0	10.1 SP1	10.1	10.0
15 May 11 (Continued)	cpri_rx_cnt_sync port Description and Frame Synchronization FSM in User Guide are Incorrect	Fixed	✓	✓	✓
	MII Interface Description in v10.1 User Guide Contains Errors	Fixed	✓	✓	—
	CPRI Protocol Version Default Value is Invalid	Fixed	✓	✓	—
	Erroneous File Names in CPRI 10.1 Testbench Description in User Guide	Fixed	✓	✓	—
	Cannot Simulate CPRI MegaCore Function in Verilog HDL	Fixed	✓	✓	—
15 Feb 11	CPU Interface Deadlocks After Attempt to Access Ethernet or HDLC Registers When MII Interface Enabled	—	Fixed	✓	✓
	Errors in .mif File Names in Auto-rate Negotiation Testbenches	—	Fixed	✓	—
	Testbench tb_altera_cpri.vhd Does Not Simulate	—	Fixed	✓	—
	Cyclone IV GX REC Master Cannot Achieve Link Synchronization	—	Fixed	✓	—
	Some MegaCore Variations Have Invalid cpri_clkout Frequency	—	Fixed	✓	—
15 Dec 10	Timing Violations in Some Device Families, Speed Grades, and Line Rates	✓	✓	✓	✓
15 Aug 10	PRBS is Not Supported in Cyclone IV GX Devices	—	—	Fixed	✓
15 Jul 10	Auto-Rate Negotiation Does Not Support 614.4 Mbps Line Rate in Cyclone IV GX Devices	—	—	Fixed	✓
	Wrong Extended Rx Delay Measurement Clock Period	—	—	Fixed	✓
	Simulation Testbench Does Not Support Cyclone IV GX Variations	—	—	Fixed	✓
	Cannot Simulate Auto-Rate Negotiation in Verilog HDL With ModelSim 6.4b or Later	—	—	Fixed	✓
	Warning Messages from Transceiver While Generating and Compiling CPRI MegaCore Function	✓	✓	✓	✓
	CPRI MegaCore Function v10.0 User Guide Does Not Contain Complete Instructions for Running v10.0 Simulation Testbench	—	—	—	✓
	CPU Interrupt Bit Always Set When Interrupts are Enabled	—	—	—	Fixed
	MII Interface Description in v9.1SP1 User Guide Contains Errors	—	—	—	Fixed
	CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link	—	—	—	Fixed
	MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances	—	—	—	Fixed
	CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1	—	—	—	Fixed
	Setup Time Violations Might Occur in Arria II GX 3072 Mbps Designs	—	—	—	Fixed
01 Apr 10	CPRI MegaCore Function Does Not Support HardCopy IV GX Devices	✓	✓	✓	✓

Hold Time Failures at Line Rate 2457.6 Mbps on Arria II GX Devices

A CPRI REC master with auto-rate negotiation enabled that targets an Arria II GX device may exhibit hold time violations when running at line rate 2457.6 Mbps.

Affected Configurations

This issue affects CPRI MegaCore functions in REC configurations with line rate 2457.6 Mbps and with auto-rate negotiation enabled that target an Arria II GX device.

Design Impact

This issue may cause hold time violations that lead to hardware failure.

Workaround

To avoid this issue, add the following line to your Quartus II Project Settings File (.qsf):

```
set_instance_assignment -name GLOBAL_SIGNAL OFF -to *rx_clkout*
```

This constraint affects the CPRI MegaCore function PCS rx_clkout clock.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

Cannot Simulate Auto-Rate Negotiation in VHDL Models that Target Arria II GZ, Cyclone IV GX, and Stratix IV GX Devices

If you generate a VHDL simulation model for your CPRI MegaCore function that targets an Arria II GZ, Cyclone IV GX, or Stratix IV GX device, you cannot use it to simulate auto-rate negotiation.

Affected Configurations

All CPRI MegaCore function VHDL simulation models with auto-rate negotiation enabled that target an Arria II GZ, Cyclone IV GX, or Stratix IV GX device

Design Impact

This issue affects simulation only.

Workaround

This issue has no workaround. To simulate auto-rate negotiation, generate and simulate a Verilog HDL simulation model.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPRI_ROUND_DELAY Register Value is Wrong by Eight Clock Cycles

The value in the rx_round_trip_delay field of the CPRI_ROUND_DELAY register is eight cycles too large. To use the register value in the calculations described in the CPRI MegaCore Function User Guide, you must first subtract eight from the value in the rx_round_trip_delay register field.

Affected Configurations

All CPRI MegaCore function variations.

Design Impact

This issue affects the accuracy of all delay calculations based on the round-trip delay value in the CPRI_ROUND_DELAY register.

Workaround

To ensure your delay calculations are accurate, subtract eight from the value in the rx_round_trip_delay field of the CPRI_ROUND_DELAY register and use this calculated value instead of the register field contents in all delay calculations.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

cpri_rx_cnt_sync port Description and Frame Synchronization FSM in User Guide are Incorrect

The description of the cpri_rx_cnt_sync port (bits [4:2] of the extended_rx_status_data bus) in the *CPRI MegaCore Function User Guide* is incorrect for CPRI MegaCore function versions 10.0 and 10.1. The description in the Extended Rx Status Signals table in Chapter 5, Signals incorrectly describes the port, and the description of the initialization sequence for the testbenches, in Chapter 7, Testbenches, incorrectly implies this port has value 0x2 when frame synchronization completes.

In addition, Figure 4-10 in Chapter 4, Functional Description is mislabeled. The state labeled XSYNC3 should instead be labeled HFNSYNC1, and the state labeled HFNSYNC should instead be labeled HFNSYNC2.

The correct description of this port tells you that the port indicates the current state number (starting from zero rather than one) among the states whose category is indicated by the cpri_rx_state port (bits [1:0] of the extended_rx_status_data bus). For example, if the value of cpri_rx_state is 2'b10, the frame synchronization machine is in an XSYNC state. The cpri_rx_cnt_sync port tells you which XSYNC state the machine is in: if cpri_rx_cnt_sync has value 2'b00, the machine is in the state XSYNC1, and if it has value 2'b01, the machine is in state XSYNC2. Refer to the frame synchronization state machine figure in Chapter 4, Functional Description, with the modifications described in this erratum.

Therefore, when cpri_rx_state has value 2'b11, cpri_rx_cnt_sync cannot have value 0x2. The frame synchronization machine has only two HFNSYNC states. After frame synchronization completes, the value of cpri_rx_cnt_sync is 3b'001, not 3b'010 as erroneously indicated in the Testbenches chapter.

Affected Configurations

All CPRI MegaCore function variations.

Design Impact

If you interpret the `cpri_rx_cnt_sync` port according to the description in the user guide, you wait for a value that will never appear to signal the HFNSYNC state of the CPRI frame synchronization machine.

Workaround

Interpret the `cpri_rx_cnt_sync` port (bits [4:2] of the `extended_rx_status_data` bus) according to this erratum rather than according to the description in the Signals chapter of the *CPRI MegaCore Function User Guide*.

Solution Status

This issue is fixed in version 11.0 of the *CPRI MegaCore Function User Guide*.

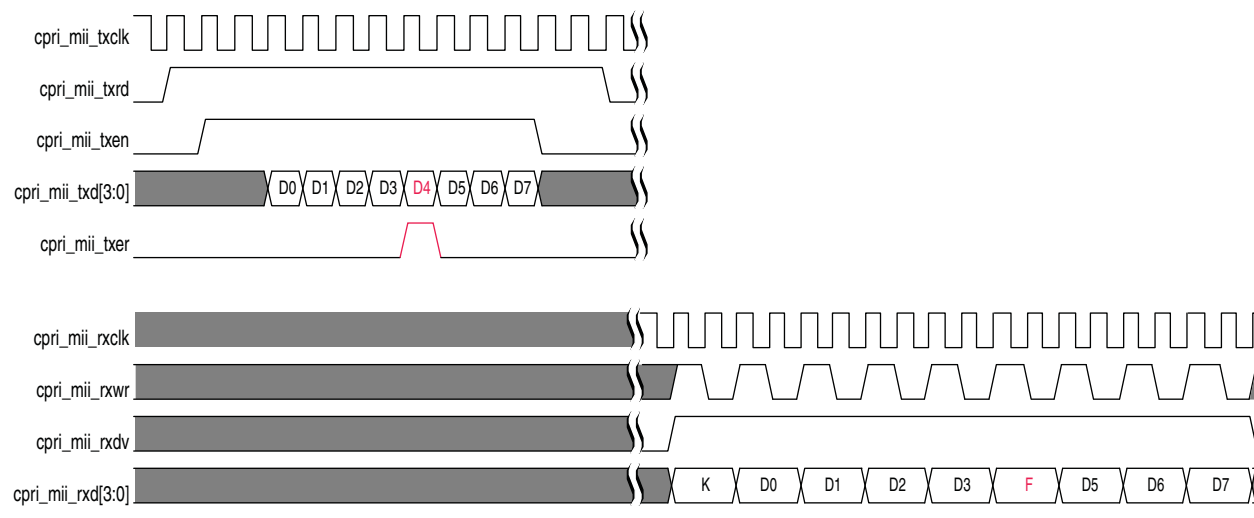
MII Interface Description in v10.1 User Guide Contains Errors

The CPRI MegaCore Function v10.1 User Guide contains an erroneous example of MII interface behavior. Figure 4-23, CPRI MII Interface Transmitter Example 1, on page 78 of the *CPRI MegaCore Function User Guide* shows input behavior that the MII interface cannot handle. Specifically, if the `cpri_mii_txen` signal toggles during transmission of a single packet, as shown in Figure 4-23, the incoming data is not transmitted correctly on the CPRI link.

You should not rely on Figure 4-23, nor any part of its explanation that describes a toggling `cpri_mii_txen` input signal. Refer instead to Figure 4-24 on the same page, CPRI MII Interface Transmitter Example 2.

Figure 4-26, CPRI MII Interface Signals on Transmitting RE or REC Master and on Receiving RE Slave, also shows this behavior. Replace Figure 4-26 on page 80 of the *CPRI MegaCore Function User Guide* with the following [Figure 6-1](#).

Figure 6-1. Corrected CPRI MII Interface Signals on Transmitting RE or REC Master and on Receiving RE Slave



Affected Configurations

This documentation issue affects all CPRI MegaCore function variations configured with the MII interface.

Design Impact

Data received on the CPRI IP core MII interface is not transmitted correctly on the CPRI link if the data originates at an external Ethernet block that toggles the `cpri_mii_txen` signal input to the CPRI IP core.

Workaround

Do not refer to Figure 4-23 in the CPRI MegaCore Function v10.1 User Guide. Instead, refer to Figure 4-24 and its description for correct behavior of an external Ethernet block.

Solution Status

This issue is fixed in version 11.0 of the *CPRI MegaCore Function User Guide*. The erroneous figure is removed.

CPRI Protocol Version Default Value is Invalid

The default value of the `tx_prot_version` field of the `CPRI_TX_PROT_VER` register is 0. However, this is not a valid value for this field. Valid values are 1 and 2. Currently, the CPRI MegaCore function recognizes the value 0 as a 1, in system configurations with two CPRI MegaCore function instances connected through a CPRI link. However, this invalid value might not be recognized as a 1 by third-party CPRI partners.

Affected Configurations

All CPRI MegaCore function variations.

Design Impact

The invalid value might not be recognized as a 1 by third-party CPRI partners. In this case, the CPRI MegaCore function and its link partner cannot achieve link synchronization.

Workaround

Immediately following system initialization, set the `tx_prot_version` field of the `CPRI_TX_PROT_VER` register to value 1 or 2.

Solution Status

This issue is fixed in version 11.0 of the CPRI MegaCore function.

Erroneous File Names in CPRI 10.1 Testbench Description in User Guide

In the Testbenches chapter of the *CPRI MegaCore Function User Guide*, in the instructions to prepare to simulate Verilog HDL files with ModelSim SE, some filename suffixes are wrong. However, note that the erratum “[Cannot Simulate CPRI MegaCore Function in Verilog HDL](#)” on page 6–7 supersedes this issue.

Affected Configurations

Testbenches simulated in Verilog HDL with ModelSim SE.

Design Impact

This issue has no design impact. It affects only the testbenches simulated in Verilog HDL with ModelSim SE.

Workaround

To fix this issue, in the user guide instructions to prepare to simulate Verilog HDL files with ModelSim SE, follow these steps.

- Replace all instances of `cpri_top_level.v` with `cpri_top_level.vo`.
- Replace all instances of `tb_altera_cpri[_<variation>].v` with `tb_altera_cpri[_<variation>].vhd`.

However, note that the erratum “[Cannot Simulate CPRI MegaCore Function in Verilog HDL](#)” on page 6-7 supersedes this issue.

Solution Status

This issue is fixed in version 11.0 of the *CPRI MegaCore Function User Guide*.

Cannot Simulate CPRI MegaCore Function in Verilog HDL

Simulation of the CPRI MegaCore function in Verilog HDL is not functional, due to an underlying Quartus II software v10.1 issue with RAM modelling in Verilog HDL.

Affected Configurations

All CPRI MegaCore functions with functional models generated in Verilog HDL.

Design Impact

This issue has no design impact. This issue affects simulation only.

Workaround

This issue has no workaround. You can generate your CPRI MegaCore function simulation model in VHDL.

Solution Status

This issue is fixed in version 11.0 of the CPRI MegaCore function.

CPU Interface Deadlocks After Attempt to Access Ethernet or HDLC Registers When MII Interface Enabled

If the application attempts to access Ethernet or HDLC registers in a CPRI MegaCore function variation with the MII interface enabled, the CPU might hang while awaiting deassertion of the `cpu_waitrequest` signal.

Affected Configurations

All CPRI MegaCore function variations with the MII interface enabled (**Include MAC block** is turned off).

Design Impact

The CPU might hang and require reprogramming.

Workaround

This issue has no workaround. You should avoid accessing the non-existent Ethernet and HDLC registers when your CPRI MegaCore function variation does not include an internal MAC block.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

In version 10.1 SP1 and beyond, accessing the non-existent Ethernet and HDLC registers no longer causes the CPRI MegaCore function to hang. Instead, the CPRI MegaCore function treats these accesses as accesses to reserved register space: write accesses are ignored and read accesses return zero values.

Errors in .mif File Names in Auto-rate Negotiation Testbenches

The Memory Initialization File (.mif) names in the ROM files included in the auto-rate negotiation testbenches do not match the generated file names. You can fix this error manually and run the testbenches.

Affected Configurations

This issue affects only the **tb_altera_cpri_autorate** and **tb_altera_cpri_c4gx_autorate** customer demonstration testbenches.

Design Impact

The **tb_altera_cpri_autorate** and **tb_altera_cpri_c4gx_autorate** customer demonstration testbenches cannot simulate.

Workaround

To avoid this issue, before simulating the **tb_altera_cpri_autorate** or **tb_altera_cpri_c4gx_autorate** testbench, edit the following files to remove the string `alt<chars>gxb` from the .mif file names:

- **rom_stratix4gx_<rate>_m.v**
- **rom_stratix4gx_<rate>_m.vhd**
- **rom_cyclone4gx_<rate>_m.v**
- **rom_cyclone4gx_<rate>_m.vhd**

The Testbenches chapter in the *CPRI MegaCore Function User Guide* tells you do this only in the .vhd files. However, this step is necessary in the .v files as well.

The **tb_altera_cpri_autorate** testbench uses the **rom_stratix4gx** files, and the **tb_altera_cpri_c4gx_autorate** testbench uses the **rom_cyclone4gx** files.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Testbench **tb_altera_cpri.vhd** Does Not Simulate

The testbench **tb_altera_cpri** does not simulate in VHDL because of an error in the **compile_vhdl.do** file. You can fix this error manually and run the testbench.

Affected Configurations

This issue affects only the **tb_altera_cpri** customer demonstration testbench in VHDL.

Design Impact

The **tb_altera_cpri** customer demonstration testbench cannot simulate in VHDL.

Workaround

To avoid this issue, before simulating the **tb_altera_cpri** testbench, follow these steps:

1. Open the testbench **compile_vhdl.do** file in a text editor.
2. Replace the line

```
vcom -work altera_mf -93 -explicit altera_mf_components.vhd  
with  
vcom -work altera_mf -93 -explicit lib/altera_mf_components.vhd
```

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Cyclone IV GX REC Master Cannot Achieve Link Synchronization

An REC master that targets a Cyclone IV GX device cannot achieve link synchronization with an RE slave. You can modify some source files to avoid the issue.

Affected Configurations

All CPRI MegaCore function REC masters that target a Cyclone IV GX device.

Design Impact

The REC master cannot achieve link synchronization.

Workaround

You can modify the source or generated files to fix this issue.

If you have write access to your IP installation files, before you generate your CPRI MegaCore function, follow these steps.

1. In a command shell, change directory to *<IP installation>/altera/cpri/src/altgx*.

2. Change directory to **614** and type the following command:

```
qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \  
cyclone4gx_614_s_tx.vhd
```

3. Change directory to **../1228** and type the following command:

```
qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \  
cyclone4gx_1228_s_tx.vhd
```

4. Change directory to **../2457** and type the following command:

```
qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \  
cyclone4gx_2457_s_tx.vhd
```

5. Change directory to **../3072** and type the following command:

```
qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \  
cyclone4gx_3072_s_tx.vhd
```

If you do not have write access to your IP installation files, you can run the same commands after you generate your CPRI MegaCore function. After generation, the same files appear in different folders in your project directory. Change directory to the appropriate folders to run the same commands.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Some MegaCore Variations Have Invalid cpri_clkout Frequency

CPRI MegaCore function variations with data rate 6.144 Gbps and with auto-rate negotiation disabled that target an Arria II GX device are generated with an invalid `cpri_clkout` frequency.

Affected Configurations

All CPRI MegaCore function variations with data rate 6.144 Gbps and with auto-rate negotiation disabled that target an Arria II GX device.

Design Impact

As a result of the invalid `cpri_clkout` frequency, the physical link cannot achieve link synchronization.

Workaround

To avoid this issue, implement one of the following two workarounds:

- Turn on auto-rate negotiation in your CPRI MegaCore function.

- Modify the source or generated files to fix this issue.

If you have write access to your IP installation files, before you generate your CPRI MegaCore function, follow these steps:

- a. Open the *<IP installation>/altera/cpri/src/altera_cpri.vhd* file in a text editor.
- b. On line 3251, replace `clk0 => tx_clkout` with `clk0 => txclk_div2`.
- c. On line 3259, replace `clk0 => rx_clkout` with `clk0 => rxclk_div2`.

If you do not have write access to your IP installation files, you can modify the top-level file after you generate your CPRI MegaCore function. After generation, the file appears in your project directory.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Timing Violations in Some Device Families, Speed Grades, and Line Rates

Timing violations may occur in CPRI MegaCore functions that target the combinations of device family, speed grade, and CPRI line rate shown in [Table 6-3](#).

Table 6-3. Device Family, Speed Grade, and Line Rate that Might Cause Timing Violations

Device Family	Speed Grade	Line Rate
Arria II GX	I3	6144 Mbps
Cyclone IV GX	I7, C7	3072 Mbps

Affected Configurations

This issue affects the CPRI MegaCore function variations shown in [Table 6-3](#).

Design Impact

Data might be lost on TX PLD-PCS paths in the CPRI MegaCore function.

Workaround

To avoid this issue, demote the TX PCS clock `tx_clkout` from a periphery or global clock to a LAB clock, by adding the following line to the Quartus II Project Settings File (`.qsf`) before compilation:

```
set_instance_assignment -name GLOBAL_SIGNAL OFF -to <variation>*tx_clkout*
```

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

PRBS is Not Supported in Cyclone IV GX Devices

CPRI MegaCore function variations that target a Cyclone IV GX device do not support generation and validation of predetermined pseudo-random sequences (PRBS) for antenna-carrier interface testing.

Affected Configurations

All CPRI MegaCore function variations that target a Cyclone IV GX device.

Design Impact

For these CPRI MegaCore function variations, you cannot use the PRBS feature for testing the antenna-carrier interfaces.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Auto-Rate Negotiation Does Not Support 614.4 Mbps Line Rate in Cyclone IV GX Devices

CPRI MegaCore function variations that target a Cyclone IV GX device cannot achieve a CPRI communication line rate of 614.4 Mbps using auto-rate negotiation.

Affected Configurations

All CPRI MegaCore function variations with auto-rate negotiation enabled that target a Cyclone IV GX device.

Design Impact

For these CPRI MegaCore function variations, auto-rate negotiation can change the CPRI communication line rate among 1228.8 Mbps, 2457.6 Mbps, and 3072.0 Mbps only.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Wrong Extended Rx Delay Measurement Clock Period

In the Synopsys Design Constraints File (.sdc) for the CPRI MegaCore function, the `clk_ex_delay` clock period is specified incorrectly for some CPRI MegaCore function variations.

Affected Configurations

All CPRI MegaCore function variations that use the default .sdc script.

Design Impact

Extended Rx delay measurement is inaccurate.

Workaround

Edit the `.sdc` with the correct values for an M/N ratio of 128/127 or 64/63. In the `create_clock` command for the `clk_ex_delay` clock, modify the `-period` parameter to the appropriate clock period value shown in [Table 6-4](#).

Table 6-4. Appropriate Clock Period Value

CPRI Line Rate (Mbps)	System Clock (MHz)	Extended Rx Delay Measurement Clock (clk_ex_delay)					
		M/N = 128/127			M/N = 64/63		
		Frequency (MHz)	Clock Period (ns)	Duty Cycle (ns)	Frequency (MHz)	Clock Period (ns)	Duty Cycle (ns)
614.4	15.36	15.24	65.617	32.809	15.12	66.138	33.069
1228.8	30.72	30.48	32.808	16.404	30.24	33.069	16.535
2457.6	61.44	60.96	16.404	8.202	60.48	16.534	8.267
3072.0	76.80	76.20	13.123	6.562	75.60	13.228	6.614
4915.2	122.88	121.92	8.202	4.101	120.96	8.267	4.134
6144.0	153.60	152.40	6.562	3.281	151.20	6.614	3.307

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Simulation Testbench Does Not Support Cyclone IV GX Variations

The demonstration testbench does not support simulation of CPRI MegaCore function variations that target a Cyclone IV GX device.

Affected Configurations

CPRI MegaCore functions that target a Cyclone IV GX device.

Design Impact

This issue has no design impact.

Workaround

None.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Cannot Simulate Auto-Rate Negotiation in Verilog HDL With ModelSim 6.4b or Later

CPRI MegaCore function variations with auto-rate negotiation enabled and with Verilog HDL output files cannot simulate successfully in the Mentor Graphics ModelSim 6.4b simulator or in later versions of this simulator.

Affected Configurations

All CPRI MegaCore function variations with auto-rate negotiation enabled and with Verilog HDL output files.

Design Impact

Simulation cannot complete for these variations using these simulators.

Workaround

Use the ModelSim 6.4a simulation tool to simulate these variations.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Warning Messages from Transceiver While Generating and Compiling CPRI MegaCore Function

While the MegaWizard Plug-In Manager is generating a functional simulation model for the CPRI MegaCore function, and again while it is compiling, several warning messages related to the transceiver are displayed. Starting in version 10.0, these messages include warnings about clear box output or design files. These messages can be ignored.

Affected Configurations

This Quartus II software issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact. These messages can be safely ignored.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

CPRI MegaCore Function v10.0 User Guide Does Not Contain Complete Instructions for Running v10.0 Simulation Testbench

The Testbenches chapter of the CPRI MegaCore Function v10.0 User Guide does not provide adequate details to run the v10.0 testbench successfully.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To run the demonstration testbenches successfully, in Step 4.b. of the instructions in the “Running the Testbenches” section of Chapter 7, Testbenches, do not copy any of the files with prefix **cycloneiv**.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPU Interrupt Bit Always Set When Interrupts are Enabled

The CPU interrupt output status signal `cpu_irq` is always asserted when the interrupt enable field, `intr_en`, of the `CPRI_INTR` register is asserted.

Affected Configurations

All CPRI MegaCore functions with CPU interrupts enabled.

Design Impact

While CPU interrupts are enabled, the `cpu_irq` signal is asserted, and cannot be cleared.

Workaround

Ignore the CPU interrupt output status signal `cpu_irq` or upgrade to the CPRI MegaCore function v10.0.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

MII Interface Description in v9.1SP1 User Guide Contains Errors

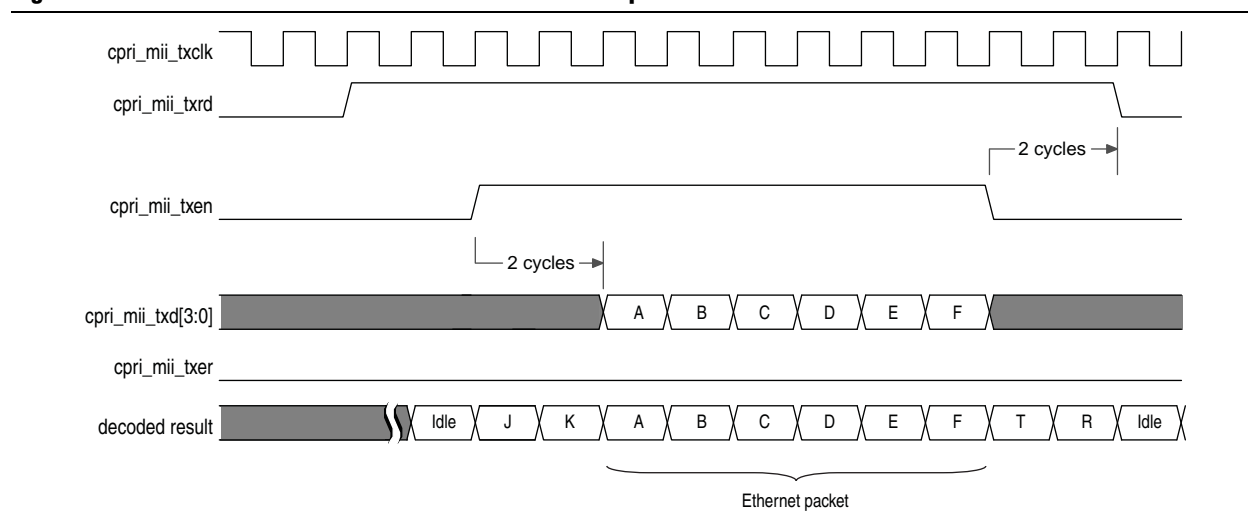
The *CPRI MegaCore Function v9.1SP1 User Guide* contains erroneous information about the MII interface. Figure 4-16 and Figure 4-17 in the *CPRI MegaCore Function User Guide* should be replaced with the figures in this erratum.

In contrast to the description in the CPRI MegaCore Function User Guide, the CPRI MII Interface transmitter inserts start-of-frame only after `cpri_mii_txen` is asserted. During the first two cycles in which `cpri_mii_txen` is asserted, the CPRI MII Interface transmitter inserts the J and K symbols in the buffer of data to be transmitted to the CPRI link, and ignores incoming data on `cpri_mii_txd`.

Typically, the external Ethernet block asserts `cpri_mii_txen` one clock cycle after `cpri_mii_txd` is asserted. If not, in each clock cycle following that first cycle, while `cpri_mii_txd` remains asserted but `cpri_mii_txen` is not yet asserted, the CPRI MII Interface transmitter inserts an Idle cycle in the buffer of data to be transmitted to the CPRI link. After `cpri_mii_txen` is asserted following the assertion of `cpri_mii_txd`, if `cpri_mii_txen` is subsequently deasserted following a cycle in which `cpri_mii_txd` remains asserted, the CPRI MII Interface transmitter assumes the external Ethernet block has reached end-of-frame, and begins insertion of the T and R nibbles.

Replace Figure 4-16 on page 56 of the CPRI MegaCore Function User Guide with the following [Figure 6-2](#).

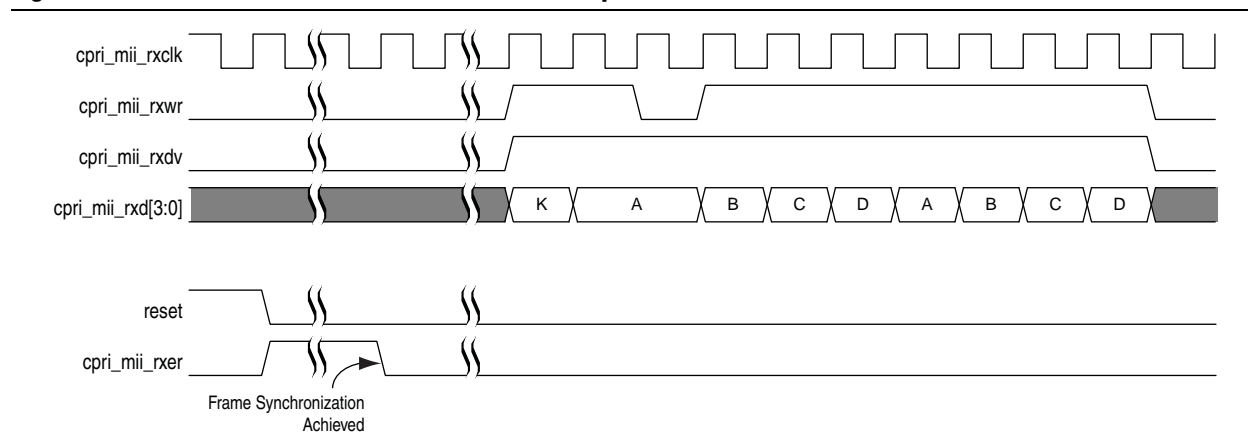
Figure 6-2. Corrected CPRI MII Interface Transmitter Example



Although [Figure 6-2](#) shows `cpri_mii_txrd` asserted continuously during transmission of an Ethernet packet on `cpri_mii_txd`, this is not always the case. The CPRI MII Interface transmitter can deassert `cpri_mii_txrd` while `cpri_mii_txen` is still asserted, to backpressure the external Ethernet block. If this happens, the Ethernet block must deassert `cpri_mii_txen` on the following cycle, to prevent the MII Interface transmitter buffer from overflowing. The `cpri_mii_txen` signal should remain deasserted until the cycle following reassertion of `cpri_mii_txrd`. If `cpri_mii_txen` is not reasserted in the cycle following the reassertion of `cpri_mii_txrd`, then an Idle cyle is inserted in the packet; therefore, the external Ethernet block must reassert `cpri_mii_txen` in the cycle following reassertion of `cpri_mii_txrd`.

The CPRI MII Interface receiver transmits the K nibble to indicate start-of-frame on the MII interface. Replace Figure 4-17 on page 57 of the CPRI MegaCore Function User Guide with the following [Figure 6-3](#).

Figure 6-3. Corrected CPRI MII Interface Receiver Example



The J nibble of the start-of-frame is consumed by the CPRI MegaCore function, and is not transmitted on the MII interface.

The corrections indicated above apply to Figure 4-18 on page 57 of the CPRI MegaCore Function User Guide as well.

Affected Configurations

This issue affects all CPRI MegaCore function variations configured with the MII interface.

Design Impact

Designs that rely on the description of the MII interface in the CPRI MegaCore Function User Guide exhibit data corruption on the MII interface.

Workaround

Use the corrected description in this erratum in designing your external Ethernet block.

Solution Status

This issue is fixed in version 10.0 of the *CPRI MegaCore Function User Guide*.

CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link

The Info link to the CPRI MegaCore Function User Guide from the CPRI MegaWizard interface does not work.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To view the CPRI MegaCore Function User Guide, open the **ug_cpri.pdf** file in your *<Quartus II v9.1 SP2 IP installation>/cpri/doc* folder, or click the CPRI MegaCore Function User Guide link on the Altera [Literature: User Guides](#) web page.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances

After you generate an instance of the CPRI MegaCore function, its transceiver is not available for editing by the ALTGX MegaWizard interface. The MegaWizard Plug-In Manager does not recognize the transceiver as an existing instance of the ALTGX megafunction.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

The MegaWizard Plug-In Manager does not recognize the CPRI transceiver as an existing instance of the ALTGX megafunction.

Workaround

This issue is caused by a copyright notice at the top of the clear-text version of the ALTGX megafunction HDL code file. You can avoid this issue by editing the clear-text file to remove the copyright notice. To remove the text that causes the problem, perform the following steps:

1. Open the HDL file for your transceiver instance in a text editor.
2. Remove the copyright notice and following blank lines. The first characters in the file should be the following line:

```
--megafunction wizard: %ALTGX%
```

3. Save the file. Now you can edit the transceiver instance using the ALTGX MegaWizard interface.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1

If the CPRI frame synchronization machine is in the XSYNC1 state and does not receive the K28.5 byte, the frame synchronization machine remains in state XSYNC1 instead of moving to state XACQ1 as it should.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

While the core is in the XSYNC1 state, the frame synchronization logic locks up until a K28.5 byte is detected.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

Setup Time Violations Might Occur in Arria II GX 3072 Mbps Designs

Designs that include a CPRI MegaCore function that runs the CPRI link at 3072 Mbps and targets an Arria II GX device, might exhibit setup time violations.

Affected Configurations

This issue affects some 3072-Mbps CPRI MegaCore functions that target an Arria II GX device.

Design Impact

You might observe hardware failures after you configure the device.

Workaround

To avoid this issue, use the Design Space Explorer for seed sweeping.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

CPRI MegaCore Function Does Not Support HardCopy IV GX Devices

The HardCopy IV GX device family is not supported by the current release of the CPRI MegaCore function.

Affected Configurations

This issue affects all CPRI MegaCore function variations that target a HardCopy IV GX device.

Design Impact

CPRI MegaCore function designs that target a HardCopy IV GX device cannot be compiled or simulated.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

Revision History

Table 7–1 shows the revision history for the CRC Compiler.



For more information about the new features, refer to the *CRC Compiler User Guide*.

Table 7–1. CRC Compiler Revision History

Version	Date	Description
11.0	May 2011	Final support for Cyclone IV GX, Cyclone IV E, and Stratix IV devices.
10.1	December 2010	Final support for Stratix IV GT devices.
10.0	July 2010	Maintenance release.

Errata

Table 7–2 shows the issues that affect the CRC Compiler v11.0, v10.1, and v10.0.



Not all issues affect all versions of the CRC Compiler.

Table 7–2. CRC Compiler Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
01 Dec 06	Testbench Directory Generated When You Create a Simulation Model	✓	✓	✓

Testbench Directory Generated When You Create a Simulation Model

When you create a simulation model, the CRC compiler automatically creates a **testbench** directory in the project directory for you. If you follow the **Running the Testbench Example** steps in the *CRC Compiler User Guide* to create the generator and checker files, another **testbench** directory is created as a subdirectory of the initial **testbench** directory, resulting in the following directory structure:

```
c:\altera\projects\crc_project\testbench\testbench
```

when the initial directory is

```
c:\altera\projects\crc_project\testbench
```

Affected Configuration

All CRC MegaCore function variations are affected.

Design Impact

This issue has no design impact.

Workaround

The **testbench** subdirectory (**testbench\testbench**) of the initial **c:\altera\projects\crc_project\testbench** directory may be deleted.

Solution Status

No change is planned currently.

Revision History

Table 8–1 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.



For more information about the new features, refer to the *DDR and DDR2 SDRAM Controller Compiler User Guide*.

Table 8–1. DDR and DDR2 SDRAM Controller Compiler Revision History

Version	Date	Description
11.0	May 2011	Maintenance release.
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.

Errata

Table 8–2 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v11.0, 10.1, and 10.0.



Not all issues affect all versions of the DDR and DDR2 SDRAM Controller Compiler.

Table 8–2. DDR and DDR2 SDRAM Controller Compiler Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	Rule Violation Warnings During Compilation	✓	✓	✓
15 July 10	Quartus Compilation Error	✓	✓	✓
	Partitioned Design Compilation Error	✓	✓	✓
15 Oct 07	Error: Can't Find the Clock Output Pins. Stop.	✓	✓	✓
01 Jul 07	ODT Launches Off System Clock	✓	✓	✓
01 Jun 06	Error Message When Recompiling a Project	✓	✓	✓
	Pin Planner HDL Syntax Error	✓	✓	✓

Rule Violation Warnings During Compilation

If you compile your designs using DDR or DDR2 SDRAM Controller version 9.1 and later, you get the following rule violation warnings:

Rule A103: Design should not contain delay chains.

Rule C104: Clock signal source should drive only clock input ports.

Rule R105: The reset signal that is generated in one clock domain and used in another clock domain should be synchronized.

Rule C106: Clock signal source should not drive registers triggered by different clock edges.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 SDRAM Controller version 9.1 and later.

Design Impact

None.

Workaround

Use the high-performance controllers with ALTMEMPHY or UniPHY instead.

Solution Status

This issue will not be fixed.

Quartus Compilation Error

Designs that target the Cyclone II devices fail to compile in version 10.0 of the Quartus II software.

Affected Configurations

This issue affects all designs that use Cyclone II devices.

Design Impact

Your design fails to compile.

Workaround

Use version 9.1 of the Quartus II software.

Solution Status

This issue will not be fixed.

Partitioned Design Compilation Error

Partitioned designs that use the DDR2 SDRAM Controller fail compilation at cke and odt pins.

Affected Configurations

This issue affects all designs that use the DDR2 SDRAM Controller.

Design Impact

Your design fails to compile.

Workaround

To compile your design successfully, in the .qsf file add the following command:

```
set_instance_assignment -name REMOVE_DUPLICATE_REGISTERS OFF -to  
"ddr2_ctrl:ddr2_ctrl_ddr_sdram|ddr2_ctrl_auk_ddr_sdram:ddr2_ctrl_auk_ddr_s  
dram_inst|auk_ddr_controller:ddr_control|cke"
```

Solution Status

This issue will not be fixed.

Error: Can't Find the Clock Output Pins. Stop.

The post-compile timing script reports the following error:

```
'Couldn't find the clock output pins. Stop.'
```

Affected Configurations

This issue affects designs using the DDR SDRAM controller, when the PLL counters have been reordered or the clocks for the DDR SDRAM interface are not on global clocks. This issue may occur automatically in the Fitter if there is pressure on global clock resources.

Design Impact

The design fails.

Workaround

Make the following two assignments:

```
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst Preserve PLL Counter Order  
On  
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst|altpll:altpll_component|_c  
lk3* Global Signal Global Clock
```



Replace the file names of the PLL with those in your DDR SDRAM controller design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

ODT Launches Off System Clock

In designs with a separate address and command clock, the ODT output launches from the system clock, not from this address and command clock.

Affected Configurations

This issue affects the following configurations:

- DDR2 SDRAM controller (not DDR SDRAM)
- ODT is turned on
- CAS latency is set to three

- The design uses a separate address and command clock and not the default system clock

Design Impact

This issue has no design impact.

Workaround

Use a CAS latency of four, which means one extra cycle of read latency, or use the DDR2 SDRAM High-Performance controller, which uses the ALTMEMPHY megafunction to transfer all the address and command outputs to the correct clock.

Solution Status

This issue will not be fixed.

Error Message When Recompiling a Project

If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

```
Error: DDR timing cannot be verified until project has been successfully compiled.
```

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

Affected Configurations

This issue affects all configurations.

Design Impact

The timing script does not verify your design.

Workaround

Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

Solution Status

This issue will not be fixed.

Pin Planner HDL Syntax Error

There is an HDL syntax error in Pin Planner-generated top-level design files that contain a DDR or DDR2 SDRAM Controller variation.

Affected Configurations

Pin Planner-generated top-level design files that use a design that contains a DDR or DDR2 SDRAM Controller variation.

Design Impact

If you import the DDR or DDR2 SDRAM Controller Pin Planner file into Pin Planner and then generate a top-level design file for your design, it contains an HDL syntax error and does not compile in the Quartus II software. You cannot use this top-level design file for IO Assignment Analysis.

Workaround

Use the IP Toolbench top-level example design and automatically assigned constraints to verify your pin and IO assignments.

Solution Status

This issue will not be fixed.

Revision History

Table 9–1 shows the revision history for the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function.



For more information about the new features, refer to the *DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP User Guide*.

Table 9–1. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Revision History

Version	Date	Description
11.0 SP1	July 2011	Maintenance release
11.0	May 2011	Added new controller features, including data-reordering capability
10.1	December 2010	Maintenance release
10.0 SP1	September 2010	Maintenance release
10.0	July 2010	<ul style="list-style-type: none"> Added information for new GUI parameters: Controller latency, Enable reduced bank tracking for area optimization, and Number of banks to track. Removed information about IP Advisor. This feature is removed from the DDR/DDR2 SDRAM IP support for version 10.0.

Errata

Table 9–2 shows the issues that affect the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP v11.0, 10.1, and 10.0.



Not all issues affect all versions of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Table 9–2. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version				
		11.0 SP1	11.0	10.1	10.0 SP1	10.0
1 Jul 11	ECC Interrupt Function Not On by Default	✓	✓	—	—	—
	ECC Registers Not Accessible from Controller Register Map	✓	✓	—	—	—
	Error Related to Incorrect Syntax of Type Conversion	✓	✓	—	—	—
	SOPC Builder and Qsys Do Not Support Full-Rate DDR with HPC I in Simulation	✓	✓	—	—	—
	Need to Manually Connect Memory Model	✓	✓	—	—	—
	VCS Simulation Fails and Reports that Module was Previously Declared	✓	✓	—	—	—
	Half Rate Bridge Not Supported in Simulation	✓	✓	—	—	—
	System Timestamp Mismatch Warning Message	✓	✓	—	—	—
	VHDL Example Driver Fails in Simulation	✓	✓	—	—	—
15 Dec 10	Resynchronization Registers Incorrectly Placed in Core instead of I/O	—	Fixed	✓	✓	—
	pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems	✓	✓	✓	—	—
	Warning Messages Reporting Ignored SDC Constraints	✓	✓	✓	—	—
	SOPC Builder Not Supported for DDR SDRAM Controller with ALTMEMPHY	✓	✓	✓	—	—
15 Sept 10	Reduced Clock Rate Specification for Column and Row I/Os	✓	✓	✓	✓	✓
15 July 10	Error in Board Settings GUI	✓	✓	✓	✓	✓
	Using Merging Feature	✓	✓	✓	✓	✓
	Memory Controller Returns Wrong Data	✓	✓	✓	✓	✓
	Refresh to Precharge Command Timing Violation	✓	✓	✓	✓	✓
	Power-Down Entry Command Timing Violation	✓	✓	✓	✓	✓
	Failure to Regenerate 9.0 Designs in Silent Mode	✓	✓	✓	✓	✓
15 May 10	Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification	✓	✓	✓	✓	✓
	DQS and DQSn Signals Generate Extra Pulse	✓	✓	✓	✓	✓
01 Apr 10	Postamble Calibration Scheme in Sequencer Violates Timing	✓	✓	✓	✓	✓
	CSR Address 0x005 and 0x006 Contents Cannot be Accessed	✓	✓	✓	✓	✓
	Half-Rate Clock Not Connected When Clock Sharing is Enabled	✓	✓	✓	✓	✓
15 Feb 10	Wrong Default Value	✓	✓	✓	✓	✓
15 Nov 09	Timing Violation In Half-Rate Bridge Enabled Designs	✓	✓	✓	✓	✓
	Generate Simulation Model Option Gets Disabled	✓	✓	✓	✓	✓
	DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation	✓	✓	✓	✓	✓
	Designs with Eight Chip Selects Fail Compilation	✓	✓	✓	✓	✓

Table 9–2. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version				
		11.0 SP1	11.0	10.1	10.0 SP1	10.0
15 Mar 09	Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	✓	✓	✓	✓	✓
01 Dec 08	SOPC Builder Does Not Recognize Decimal Points	✓	✓	✓	✓	✓
15 May 08	RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected	✓	✓	✓	✓	✓
	Gate Level Simulation Fails	✓	✓	✓	✓	✓
	VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected	✓	✓	✓	✓	✓
	Memory Presets Contain Some Incorrect Memory Timing Parameters	✓	✓	✓	✓	✓
15 Oct 07	Mimic Path Incorrectly Placed	✓	✓	✓	✓	✓
01 Dec 06	Simulating with the NCSim Software	✓	✓	✓	✓	✓
	Simulating with the VCS Simulator	✓	✓	✓	✓	✓

ECC Interrupt Function Not On by Default

When you turn on the **Enable Error Detection and Correction Logic** option, the ECC Interrupt function is not turned on by default.

Affected configurations

This issue affects all configurations using the 11.0 version of the high-performance controller II with the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

When a single-bit or double-bit error occurs, the ECC logic does not trigger the ecc_interrupt signal.

Workaround

There is no workaround for this issue for VHDL designs.

For Verilog designs, the workaround is to open the <variation_name>_alt_mem_ddrx_controller_top.v file in an editor and change the line:

```
.CFG_ENABLE_INTR(CFG_ENABLE_INTR),
```

to

```
.CFG_ENABLE_INTR(CTL_ECC_ENABLED),
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

ECC Registers Not Accessible from Controller Register Map

When you turn on the **Enable Error Detection and Correction Logic** option, the ECC control register, ECC status register, and ECC error address register are not accessible from the controller register map.

Affected configurations

This issue affects all configurations using the 11.0 version of the high-performance controller II with the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

You are unable to access the ECC control register, ECC status register, or ECC error register in the controller register map.

Workaround

There are two workaround options for this issue.

Option 1:

Enable the **Configuration and Status Register Interface** when you enable the **Error Detection and Correction Logic** option.

Option 2 (applicable to Verilog designs only):

Open the `alt_mem_ddrx_controller_st_top.v` file in an editor and change the line:

```
if (CTL_CSR_ENABLED == 1) begin
...
    .MEM_IF_DQS_WIDTH      (
CFG_MEM_IF_DQS_WIDTH      )
) register_control_inst (

to

if (CTL_CSR_ENABLED == 1) || CTL_ECC_CSR_ENABLED == 1) begin
...
    .MEM_IF_DQS_WIDTH      (
CFG_MEM_IF_DQS_WIDTH      ),
    .CTL_CSR_ENABLED       (
CTL_CSR_ENABLED           ),
    .CTL_ECC_CSR_ENABLED   (
CTL_ECC_CSR_ENABLED       )
) register_control_inst (
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Error Related to Incorrect Syntax of Type Conversion

When you attempt to simulate a VHDL simulation model with VCS MX using NativeLink, compilation fails and reports an error message relating to incorrect syntax of type conversion.

Affected configurations

This issue affects all VHDL designs targeting DDR, DDR2, or DDR3 with the high-performance controller II (HPC II) and ALTMEMPHY.

Design Impact

Compilation fails.

Workaround

Use Verilog rather than VHDL.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

SOPC Builder and Qsys Do Not Support Full-Rate DDR with HPC I in Simulation

SOPC Builder and Qsys do not support full-rate DDR designs using the high-performance controller (HPC I) in simulation. DDR2 designs are supported.

Affected configurations

This issue affects all full-rate DDR designs with the high-performance controller (HPC), generated with SOPC Builder or with Qsys.

Design Impact

The design fails during calibration.

Workaround

There is no workaround for this issue.

Solution Status

This issue will not be fixed.

Need to Manually Connect Memory Model

When you attempt to generate a DDR with ALTMEMPHY design with Qsys and set the **Create testbench Qsys system** option to any value other than **None**, the system fails to connect a memory model to the Qsys-generated testbench.

Affected configurations

This issue affects all ALTMEMPHY designs targeting DDR memory devices.

Design Impact

Simulation does not complete properly.

Workaround

Manually instantiate the generated memory model

(`<instance_name>_mem_model.v/.vhd`) in the Qsys-generated testbench
(`<instance_name>_tb.v/.vhd`).

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

VCS Simulation Fails and Reports that Module was Previously Declared

If you set VCS as your simulator and attempt to simulate your high-performance controller II (HPC II)-based design with NativeLink, the VCS simulation fails and reports that the module was previously declared.

Affected configurations

This issue affects all high-performance controller II (HPC II)-based IP designs with ALTMEMPHY.

Design Impact

Compilation fails in VCS.

Workaround

The workaround for this issue is to perform the following steps, before running the simulation:

1. Open the `<variation_name>.v` file in an editor.
2. In the `<variation_name>.v` file, find the following text:
`// IPFS_FILES: <files list>;`
3. Remove the entire file list by replacing the text located in step 2 with the following text: `// IPFS_FILES: ;`

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Half Rate Bridge Not Supported in Simulation

If you open an IP design created in version 10.1 of the Quartus II software in version 11.0 and enable the Half Rate Bridge feature, the design may fail in simulation.

Affected configurations

This issue affects all 10.1 designs opened in the Quartus II software version 11.0.

Design Impact

Simulation fails.

Workaround

Do not enable the Half Rate Bridge feature.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

System Timestamp Mismatch Warning Message

A warning message similar to the following might be displayed during IP generation with SOPC Builder: `system timestamp mismatch - connected: 1301987588`.

Affected configurations

All ALTMEMPHY-based systems generated with SOPC Builder.

Design Impact

This issue has no design impact.

Workaround

You may ignore the displayed message.

Solution Status

This issue will not be fixed.

VHDL Example Driver Fails in Simulation

The VHDL example driver for designs using the high-performance controller (HPC) fails to simulate.

Affected configurations

This issue affects all ALTMEMPHY-based designs using the high-performance controller, and targeting VHDL.

Design Impact

The VHDL example driver fails to compile in VCS/VCSMX and hence cannot simulate.

Workaround

The workaround for this issue is to use the Verilog example driver.

Solution Status

This issue will not be fixed.

Resynchronization Registers Incorrectly Placed in Core instead of I/O

For designs targeting Arria II GX devices, the Quartus II software incorrectly places resynchronization registers in the core instead of the I/O.

Affected configurations

This issue affects designs targeting Arria II GX devices and using the DDR or DDR2 SDRAM Controllers with ALTMEMPHY IP.

Design Impact

Possible intermittent data corruption of the last word in a burst.

Workaround

For Quartus II software versions 10.1 and 10.0SP1, download and install the Quartus II software patch described in the solution available here:

http://www.altera.com/support/kdb/solutions/rd12132010_638.html.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems

For systems generated with Qsys, the `<variation_name>_pin_assignments.tcl` script does not assign correct pin names. This situation occurs because the entity name assigned by Qsys is not yet known at generation time when the `<variation_name>_pin_assignments.tcl` script is generated.

Affected configurations

This issue affects all configurations.

Design Impact

Your design fails to simulate and does not work in hardware.

Workaround

After generating your IP core, edit the `<variation_name>_pin_assignments.tcl` script and change the `set instance_name` line to specify the correct name of your controller instance.

Solution Status

This issue will not be fixed.

Warning Messages Reporting Ignored SDC Constraints

During compilation of a Qsys-generated IP core, the TimeQuest Timing Analyzer may display warning messages indicating that SDC constraints are being ignored. These messages appear because TimeQuest reads the `altera_avalon_half_rate_bridge_constraints.sdc` file even though the Half Rate Bridge feature is not used.

Affected configurations

This issue affects all Qsys-generated configurations.

Design Impact

This issue has no design impact.

Workaround

To prevent display of the warning messages, remove the `altera_avalon_half_rate_bridge_constraints.sdc` file from the project and from any `.qip` file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

SOPC Builder Not Supported for DDR SDRAM Controller with ALTMEMPHY

SOPC Builder does not support the DDR SDRAM Controller with ALTMEMPHY in version 10.1. The DDR2 SDRAM Controller with ALTMEMPHY is supported.

Affected configurations

This issue affects all configurations.

Design Impact

Your design fails.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

Reduced Clock Rate Specification for Column and Row I/Os

Commencing with the Quartus II software version 10.0 SP1, the clock rate specification for column and row I/Os is decreased from 150MHz to 133MHz for full-rate DDR2 IP cores on Cyclone IV E I8L devices with vcc=1.0V. This reduction in specification is due to changes associated with finalized timing models.

Affected Configurations

This issue affects all configurations.

Design Impact

The maximum clock rate for column and row I/Os is decreased.

Workaround

Do not use the IP core with column and row I/Os greater than 133MHz in full-rate mode on Cyclone IV E I8L devices with vcc=1.0V.

Designs already using Cyclone IV E I8L devices with vcc=1.0V with full-rate DDR2 SDRAM at 150MHz (the previous clock rate specification) which pass timing in the Quartus II software version 10.0SP1 and later should continue to work, as long as you accurately populate the Board Settings panel in the MegaWizard and you correctly enter board trace models representative of the system in the Pin Planner.

Solution Status

This issue will not be fixed.

Error in Board Settings GUI

The following board settings errors occur in the ALTMEMPHY MegaWizard interface:

- For Cyclone IV E and Cyclone IV GX designs, the single-rank board presets are used even if you specify more than one chip select.
- For Stratix III designs, the board parameters are editable but cannot be used for timing analysis.

Affected Configurations

This issue affects all designs that target the Cyclone IV or Stratix III devices.

Design Impact

Your design may be parameterized wrongly.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Using Merging Feature

When you generate designs with DDR or DDR2 high-performance controller II (HPC II), the merging feature is turned off by default. If your traffic exercises pattern that you can merge, you should turn on merging. Turning merging on may affect f_{MAX} performance.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture in version 10.0 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Design Impact

If you can merge traffic when you turn on the merging feature, there is a performance improvement.

Workaround

To turn on the command merging feature, follow these steps:

1. Open the `<variation_name>_alt_ddrx_controller_wrapper.v` file.
2. Search for the `ENABLE_BURST_MERGE` parameter.
3. Change the value from 0 to 1.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Memory Controller Returns Wrong Data

For designs that use the DDR or DDR2 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder, the memory controller returns incorrect data. When you initialize the memory content with the initialization data file, the fetched memory content does not match the initialization data file. This issue does not affect operation in hardware.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder.

Design Impact

Your design fails to simulate.

Workaround

Select **CHIP-BANK-ROW-COL** for the **Local-to-Memory Address Mapping** option instead.

Solution Status

This issue will not be fixed.

Refresh to Precharge Command Timing Violation

Designs that use the DDR or DDR2 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.
2. Locate the following command:

```
cs_can_precharge_all [w_cs] = chip_idle;
```

and change to:

```
cs_can_precharge_all [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Power-Down Entry Command Timing Violation

Designs that use the DDR or DDR2 HPC II architecture with the **Enable Auto Power Down** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture with the **Enable Auto Power Down** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.

2. Locate the following command:

```
always @ (*)
begin
    cs_can_power_down [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
end

and change to:
always @ (posedge ctl_clk or negedge ctl_reset_n)
begin
    if (!ctl_reset_n)
        cs_can_power_down [w_cs] <= 1'b0;
    else
        cs_can_power_down [w_cs] <= power_saving_enter_ready [w_cs] & chip_idle;
    end
end
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Failure to Regenerate 9.0 Designs in Silent Mode

If you regenerate your version 9.0 designs in silent mode, the controller is defaulted to the HPC II architecture and triggers a “memory burst length” error.

Affected Configurations

This issue affects all version 9.0 configurations.

Design Impact

Your design fails to generate successfully.

Workaround

Open your design in version 10.0 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP, and regenerate your design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification

The maximum clock rate for Cyclone III speed grades supporting full-rate DDR2 SDRAM on column I/Os are downgraded for version 9.1 and later. The maximum clock rate is downgraded because the Quartus II tool is unable to achieve push-button placement at the faster clock rates with DDR2 SDRAM high-performance controller II (HPC II).

Table 9-3 shows the downgraded specifications for the Quartus II software version 9.1.

Table 9-3. Full-Rate DDR2 SDRAM Support for Cyclone III Devices

Memory Standard	Device	Speed Grade	Maximum Full-Rate Clock Rate (MHz)
			Column I/O (Single Chip Select)
DDR2 SDRAM	Cyclone III	C6	167 (1)
		C7	150 (2)
		C8, I7, A7	150 (1)

Notes to Table 9-3:

- (1) You need 267-MHz memory component speed grade when using class I I/O standard and 333-MHz memory component speed grade when using class II I/O standard.
- (2) You need 200-MHz memory component speed grade.

Affected Configurations

This issue affects all designs that use full-rate DDR2 SDRAM with HPC II architecture and target the Cyclone III devices. If you are using DDR2 SDRAM with HPC architecture, you are not affected by this downgrade.

Design Impact

There is no design impact.

Workaround

To achieve higher clock rates, refer to the solution provided at http://www.support/kdb/solutions/rd05112010_783.html.

Solution Status

This issue will be fixed in a future version of the DDR2 Controller with ALTMEMPHY IP.

DQS and DQSn Signals Generate Extra Pulse

The DQS and DQSn signals generate an extra pulse after a write for designs that use the half-rate DDR or DDR2 SDRAM with HPC architecture.

Because the controller asserts the DM pin high after the write burst, the extra pulse does not cause any incorrect data to be written into the memory.

Affected Configurations

This issue affects all designs that use half-rate DDR or DDR2 SDRAM with HPC architecture and target Arria II GX, Stratix III, or Stratix IV devices.

Design Impact

If your board is not using DM pins, incorrect data may be written into the memory.

Workaround

Use the HPC II architecture instead.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Postamble Calibration Scheme in Sequencer Violates Timing

For DDR memory interfaces with low frequency, the postamble calibration scheme in the sequencer violates the refresh memory timing parameter, breaching the JEDEC specifications.

Affected Configurations

This issue affects all designs with DDR SDRAM controller using the following frequencies and devices:

- Frequency between 110 and 120 MHz for Arria II GX devices.
- Frequency between 100 and 110 MHz for Stratix II devices.
- Frequency below 133 MHz frequency for Stratix III and Stratix IV devices.

Design Impact

Your design fails to simulate.

Workaround

Reduce the initial postamble latency by performing the following steps:

1. Open *<variation name>_phy_alt_mem_phy.v* file.
2. Search for the POSTAMBLE_INITIAL_LAT parameter.
3. Subtract a few cycles off from the current value.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

CSR Address 0x005 and 0x006 Contents Cannot be Accessed

Designs that use the DDR or DDR2 HPC II architecture with the **Enable Configuration and Status Register Interface** option turned on, cannot access the CSR address 0x005 and 0x006 contents.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 high-performance controller II architecture with the **Enable Configuration and Status Register Interface** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To access the CSR address 0x005 and 0x006 contents, perform the following steps:

1. Open `<variation name>_controller_phy.v` file.
2. Search for the following debug ports under the `<variation name>_phy` instantiation.
 - `dbg_clk` (Clock)
 - `dbg_addr` (Address)
 - `dbg_cs` (Chip select)
 - `dbg_waitrequest` (Wait request)
 - `dbg_wr` (Write request)
 - `dbg_wr_data` (Write data)
 - `dbg_rd` (Read request)
 - `dbg_dr_data` (Read data)
3. Export these ports into `<variation name>_example.v` file.
4. Use the Avalon-MM protocol to access the CSR address 0x005 and 0x006 contents through the debug ports.

Solution Status

This issue will not be fixed.

Half-Rate Clock Not Connected When Clock Sharing is Enabled

If you generate a DDR or DDR2 controller with the **High Performance Controller II** and **Multiple Controller Clock Sharing** options enabled in SOPC Builder, the half-rate clock is not connected.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Multiple Controller Clock Sharing** option enabled in SOPC Builder.

Design Impact

The internal half-rate bridge for the sharing PLL controller does not function.

Workaround

To connect the half-rate clock, perform the following steps:

1. Edit the sharing PLL controller top-level file to include the half-rate clock input port as in the following example:
 - Verilog HDL

```

module <variation name> (

    sys_clk_in,
    sys_half_clk_in,
    soft_reset_n,

    input sys_clk_in;
    input    sys_half_clk_in;
    input soft_reset_n;

    .sys_clk_in(sys_clk_in),
    .sys_half_clk_in(sys_half_clk_in),
    .soft_reset_n(soft_reset_n),

```

■ VHDL

```

ENTITY <variation name_master> IS
PORT (

    sys_clk_in  : IN STD_LOGIC;
    sys_half_clk_in    : IN STD_LOGIC;
    soft_reset_n      : IN STD_LOGIC;

    COMPONENT <variation name>_controller_phy
    PORT (

        sys_clk_in  : IN STD_LOGIC;
        sys_half_clk_in    : IN STD_LOGIC;
        soft_reset_n      : IN STD_LOGIC;

```

```

        sys_clk_in => sys_clk_in,
        sys_half_clk_in => sys_half_clk_in,
        aux_full_rate_clk => aux_full_rate_clk,

```

2. Edit the SOPC top-level file to connect the half-rate clock from the source to the sharing controller as in the following example:

■ Verilog HDL

```

<variation name> the_<variation name>
(

    .soft_reset_n (clk_0_reset_n),
    .sys_half_clk_in    ( <variation
name_master>_aux_half_rate_clk_out),

```

```
.sys_clk_in    (<variation name_master>_phy_clk_out)
```

■ VHDL

```
component <variation name> is
port (
-- inputs:

signal soft_reset_n : IN STD_LOGIC;
signal sys_half_clk_in : IN STD_LOGIC;
signal sys_clk_in : IN STD_LOGIC;

the_<variation name> : <variation name>
port map(

soft_reset_n => clk_0_reset_n,
sys_half_clk_in => out_clk_<variation name_master>_aux_half_rate_clk,
sys_clk_in => internal_<variation name_master>_phy_clk_out
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Wrong Default Value

If you generate the core targeting a Cyclone IV E device with the high-performance controller architecture, without creating a new project first, the MegaWizard Plug-In Manager selects the default speed grade and clock frequency values that are not supported. If you generate the core, "The given combination of PLL input and output cannot be synthesized." error message appears.

Affected Configurations

This issue affects all designs that use the high-performance controller architecture targeting Cyclone IV E devices.

Design Impact

Your system cannot be generated.

Workaround

Create a new project and select the device first before generating the core. Make sure to specify the speed grade to a value higher than 8, and the clock frequency to a value higher than 200 MHz.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Timing Violation In Half-Rate Bridge Enabled Designs

Timing violation occurs during TimeQuest timing analysis for designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on.

Affected Configurations

This issue affects all designs that use the high-performance II controller architecture with the **Enable Half Rate Bridge** option turned on.

Design Impact

Timing violation occurs during compilation in the TimeQuest timing analyzer.

Workaround

Open the `altera_avalon_half_rate_bridge_constraints.sdc` file in your project directory, and edit the `slow_clock` variable and add `derive_pll_clocks`.

■ Full-rate design

```
derive_pll_clocks  
set slow_clk "*" | altpll_component | auto_generated | pll1 | clk[1]"
```

■ Half-rate design

```
derive_pll_clocks  
set slow_clk "*" | altpll_component | auto_generated | pll1 | clk[0]"
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Generate Simulation Model Option Gets Disabled

The **Generate simulation model** option gets disabled after every generation.

Affected Configurations

This issue affects all configurations.

Design Impact

The simulation model for your design is not generated for the second time.

Workaround

Turn on the **Generate simulation model** option each time you want to generate a simulation model.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation

Designs that use the full-rate DDR SDRAM high-performance controller in AFI mode with a memory burst length of 2 fail to simulate.

Affected Configurations

This issue affects all designs that use DDR SDRAM high-performance controller in full-rate mode with a memory burst length of 2.

Design Impact

As the generated memory model does not support memory burst length of 2, your design fails to simulate.

Workaround

Use a vendor memory model instead.

Solution Status

This issue will not be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

Designs with Eight Chip Selects Fail Compilation

Designs that use eight chip selects with the high-performance controller architecture fail to compile.

Affected Configurations

This issue affects all designs that use eight chip selects with the high-performance controller architecture.

Design Impact

Your design fails to compile.

Workaround

In the MegaWizard interface, select **High Performance Controller II** as your controller architecture.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR or DDR2 SDRAM high-performance controllers do not work with the **Enable Error Detection and Correction Logic** option turned on.

Affected Configurations

This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers that have the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

Your design does not work properly in both simulation and hardware after the subsequent reset.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

SOPC Builder Does Not Recognize Decimal Points

If you assign the PLL clock with a value with decimals, SOPC Builder takes only the whole number and does not recognize the value after the decimal point. When you generate the system, the “The PLL reference clock of <value> does not match the clock frequency input to refclk” error message appears.

Affected Configurations

This issue affects all designs that have a PLL clock value with decimals.

Design Impact

Your system cannot be generated.

Workaround

Ignore the error message, and generate the system by holding down the Ctrl key on the keyboard while clicking **Generate** in SOPC Builder.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected

The example testbench RTL simulation may not simulate correctly when a dedicated memory clock phase is selected because clock net delay between the PLL and the clock output pins is not modelled in the RTL.

Affected Configurations

This issue affects designs that enable the **Use dedicated PLL outputs to drive memory clocks** option and set a value for the **Dedicated memory clock phase** parameter.

Design Impact

The design does not simulate correctly.

Workaround

Add MEM_CLK_DELAY to clk_to_ram signal at example top-level testbench, to compensate for the on-chip clock net delay to mem_dqs which is not present in the RTL simulation.

```
parameter DED_MEM_CLK = 1;
parameter real DED_MEM_CLK_PHASE = <value for dedicated memory clock phase>
parameter real mem_clk_ratio = ((360.0DED_MEM_CLK_PHASE)/360.0);
parameter MEM_CLK_DELAY = mem_clk_ratio*CLOCK_TICK_IN_PS * (DED_MEM_CLK ? 1 : 0);
wire clk_to_ram0, clk_to_ram1, clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram2 = clk_to_sdram[0];
assign #(MEM_CLK_DELAY/4.0) clk_to_ram1 = clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram0 = clk_to_ram1;
assign #((MEM_CLK_DELAY/4.0)) clk_to_ram = clk_to_ram0;
//Replace testbench clk_to_ram assignment by adding MEM_CLK_DELAY
//assign clk_to_ram = clk_to_sdram[0];
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Gate Level Simulation Fails

Gate level simulation of the example design and example testbench fails when **Use differential DQS** is enabled in the DDR2 High-Performance Controller.

Affected Configurations

This issue affects DDR2 SDRAM High-Performance Controller designs in Stratix III and Stratix IV devices that have the **Use differential DQS** option enabled.

Design Impact

Gate level simulation of the example design does not behave correctly.

Workaround

You can use the following options:

1. To connect dqs_n example top-level design:

- .mem_dqsn(mem_dqsn)
- 2. To connect dqsn in memory model:
- .DQSN mem_dqsn[index])

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM Controller with ALTMEMPHY IP.

VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected

VHDL generated sequencer block for CAS latency 2.0 and 2.5 designs using DDR SDRAM High-Performance Controller results in simulation failure. The issue is due to delta cycle delays on a clock net.

Affected Configurations

This issue affects DDR SDRAM High-Performance Controller CAS latency 2.0 and 2.5 designs.

Design Impact

This issue only affects simulation on VHDL and does not affect the functionality of the design.

Workaround

To work around this issue, follow these steps:

1. Open the `<variation_name>_phy.vho` file in the project directory.
2. Search for the `altsyncram` instantiation for the postamble block (this can be done by searching for " altsyncram" —note the white space). This should be the `altsyncram` component with a label that includes the word "postamble".
3. Search for the signal that is attached to the `clock1` port to find the point in the design where this signal is assigned to (in a test case, this is on line 4043).

```
wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1
```

4. Change the assignment as shown. The signal inside `not(..)` should be the same as the signal on `clock0` port of a second instance of the `altsyncram` component which is associated to the read datapath (with "read_dp" in the label).

```
wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1 <= not
(wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_clock_reset_sii_clk_<variation_name>_phy_alt_mem_phy_pll_sii_pll_19462_c4);
```



This step removes a delta delay for simulation but leaves the code unchanged. The right side of the assignment above is taken as the right side of the assignment to the signal which is previously assigned to the

"wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1" signal.

5. If the <variation_name>_phy component is recompiled in your simulator, the design should now pass.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

Memory Presets Contain Some Incorrect Memory Timing Parameters

The memory presets contain incorrect data for the tDSa and tDHa memory timing parameters.

Affected Configurations

This issue affects all configurations.

Design Impact

Timing analysis results for write and address/command paths may be incorrect.

Workaround

Make sure that the memory timing parameters in the MegaWizard Plug-In Manager match the datasheet of the target memory device. The output edge rate and the use of single-ended versus differential DQS may affect certain memory parameters.

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM Controller with ALTMEMPHY IP.

Mimic Path Incorrectly Placed

The Quartus II software may fail to place the mimic path correctly. The report timing script then indicates a timing setup failure on the mimic path.

Affected Configurations

This issue affects all designs.

Design Impact

Your design may fail.

Workaround

Manually edit the following parameter in the auto-generated Synopsis design constraint (.sdc) script to correct the timing analysis:

```
mimic_shift
```

Add a value of at least the worst case failed slack to the value already stated in the Synopsis design constraint file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Simulating with the NCSim Software

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the -relax switch for all calls to the VHDL analyzer.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Simulating with the VCS Simulator

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

The following workarounds exist.

VHDL

Change the following code:

- In file *<variation name>_example_driver.vhd*, change all when statements between lines 333 and 503 from when `std_logic_vector'("<bit_pattern>")` to when `"<bit_pattern>"`.
- In file *testbench\<example name>_tb*, change line 191 from signal `zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0');`

Verilog HDL

No changes are necessary. Calls to the Verilog analyzer sets the +v2k switch to enable Verilog 2000 constructs.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Revision History

Table 10–1 shows the revision history for the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.



For more information about the new features, refer to the *DDR2 and DDR3 SDRAM Controller with UniPHY IP User Guide*.

Table 10–1. DDR2 and DDR3 SDRAM Controller with UniPHY Revision History

Version	Date	Description
11.0 SP1	July 2011	Added quarter-rate support and 800MHz support for DDR3
11.0	May 2011	<ul style="list-style-type: none"> Added new controller features, including data-reordering capability Added support for DDR3L on Stratix V devices—the same specification as DDR3, but a low-power version using 1.35 V I/Os Added support for optional new efficiency monitor and protocol checker in UniPHY EMIF toolkit
10.1	December 2010	<ul style="list-style-type: none"> Added preliminary support for Arria II GZ Added full-rate DDR2 support Added DDR2 and DDR3 RDIMM support Added new generated directory structure Added new OCT Sharing Interface feature Added External Memory Interface Toolkit
10.0	July 2010	First release

Errata

Table 10–2 shows the issues that affect the DDR2 and DDR3 SDRAM Controller with UniPHY IP core v11.0, v10.1 and v10.0.

Table 10–2. DDR2 and DDR3 SDRAM Controller with UniPHY Errata (Part 1 of 3)

Added or Updated	Issue	Affected Versions			
		11.0 SP1	11.0	10.1	10.0
15 Jul 11	Error Migrating Design from 11.0 to 11.0 SP1	✓	—	—	—
	Non-leveled DDR2 Topology Fails Timing with Stratix V Devices	✓	—	—	—
	Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations	✓	—	—	—
	Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error	✓	—	—	—

Table 10–2. DDR2 and DDR3 SDRAM Controller with UniPHY Errata (Part 2 of 3)

Added or Updated	Issue	Affected Versions			
		11.0 SP1	11.0	10.1	10.0
1 Jul 11	ECC and CSR Design Fail Timing	✓	✓	—	—
	VHDL-Generated Fileset Can Encounter Synthesis Problems	✓	✓	—	—
	UniPHY CSR Ports Not Functioning Correctly	Fixed	✓	—	—
	User Guide Contains Imprecise Clock Information	✓	✓	—	—
	UniPHY IP Generation Fails if Quartus II Path Contains a Space	✓	✓	—	—
	Efficiency Monitor Latency Values Are Incorrect	✓	✓	—	—
	Memory Controller Uses 1T Memory Timing	✓	✓	—	—
	Multi-cast Write Control Not Supported	Fixed	✓	—	—
	Simulation Fails When Enable Auto Error Correction Option Enabled	Fixed	✓	—	—
	ECC and CSR Designs Fail in Simulation or Hardware	Fixed	✓	—	—
	Example Project Fails to Simulate When HardCopy Compatibility Enabled	✓	✓	—	—
	NativeLink RTL Simulation May Fail	Fixed	✓	—	—
	Simulation Fails for Memory Additive CAS Latency Settings > 0	✓	✓	—	—
	Error Messages in ModelSim Flow for Eclipse	✓	✓	—	—
	ModelSim Waveform Viewer Shows Only clk and reset Signals	Fixed	✓	—	—
	PLL Master Required for Simulation of PLL Slave	✓	✓	—	—
	Minimum Pulse Width Timing Failure	Fixed	✓	—	—
	Efficiency Monitor Statistics Incorrect for Initial Sample	✓	✓	—	—
	Simulation Fails with “Undefined System Task Call” Error	✓	✓	—	—
	Unable to Directly Recompile 10.1 Design in 11.0	✓	✓	—	—
	Using UniPHY-based Memory IP with SOPC Builder	✓	✓	—	—
	Using Avalon-MM Traffic Generator and BIST Engine	✓	✓	—	—
	Fitter Error When Compiling DDR2 Designs Below 240MHz	✓	✓	—	—
	Simulation Fails when Generating VHDL for Designs Using Nios II-based Sequencer	✓	✓	—	—
	Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys	✓	✓	—	—
	Conduit Error Messages Displayed in Qsys	✓	✓	—	—
	DDR3 ODT Fails in Simulation with Denali	Fixed	✓	—	—
	EMIF Toolkit Reports Incorrect CAS Latency for 10.1 IP Opened in 11.0	✓	✓	—	—
	Example Design Simulation May Fail in NC Sim	✓	✓	—	—
	Must Enable Support for Nios II ModelSim Flow in GUI	✓	✓	—	—
	Example Design Can Fail For Certain Parameterizations	✓	✓	—	—
	Example Design Without DM Pins Enabled Will Fail	✓	✓	—	—
	Simulation of Example Designs Can Fail or Produce Warnings	✓	✓	—	—
	Compilation of a UniPHY Example Design Can Produce Warnings	✓	✓	—	—
15 Jan 11	Error in Graphical Display of DQ Calibration Margin in EMIF Toolkit	✓	✓	✓	—

Table 10–2. DDR2 and DDR3 SDRAM Controller with UniPHY Errata (Part 3 of 3)

Added or Updated	Issue	Affected Versions			
		11.0 SP1	11.0	10.1	10.0
15 Dec 10	NativeLink Simulation fails for VHDL Output	✓	✓	✓	—
	NativeLink Simulation fails for VHDL Output	—	—	—	✓
	Timing-related Warning Messages When Sharing PLLs on Stratix V Devices	—	Fixed	✓	—
	Devices Faster than 533MHz Require Manual Derating	—	Fixed	✓	—
	Reset Synchronizer May Cause Design to Fail Timing	✓	✓	✓	—
	Compilation Fails if Synthesis Fileset is Mixed with Example Project Files	—	Fixed	✓	—
	Warning Messages Displayed When Compiling for Stratix V Devices	✓	✓	✓	—
	Cannot Launch MegaWizard Plug-In Manager by Opening Example Design	✓	✓	✓	—
	Example Design May Not Compile for IP Cores from Earlier Versions	—	Fixed	✓	—
	SOPC Builder-generated Systems Cannot Serve as Top-Level Design	—	Fixed	✓	—
	Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices	✓	✓	✓	—
15 Aug 10	Incorrect Clock Uncertainty	—	Fixed	✓	✓
	User Guide Contains Incorrect Clock Information	✓	✓	✓	✓
15 July 10	Using Burst Merging Feature	✓	✓	✓	✓
	Autoprecharge Feature is Not Available	✓	✓	✓	✓
	Global Signal Assignments Not Applied	✓	✓	✓	✓
	BSF File Not Generated	—	—	Fixed	✓
	Selecting VHDL Gives a Verilog HDL IP Core	—	—	Fixed	✓
	Designs Without Leveling Fail in Stratix V Devices	—	—	Fixed	✓
	Quartus II Software Cannot Read .mif File for PLL	✓	✓	✓	✓
	Example Design Fails as a Slave	—	—	Fixed	✓
	Simulation Fails in Riviera	✓	✓	✓	✓
	Simulation Fails—PLL Clocks Out of Synchronization	✓	✓	✓	✓
	SOPC Builder Designs Suffer Low Efficiency	—	Fixed	✓	✓

Error Migrating Design from 11.0 to 11.0 SP1

Attempts to migrate an 11.0 design to 11.0 SP1 fails and displays an error message.

Affected configurations

This issue affects designs with the CSR port or ECC enabled.

Design Impact

Migration fails, with an error message indicating that a specified value is outside the master's address range.

Workaround

The workaround for this issue is to open the .v file in an editor and change the value of CSR_ADDR_WIDTH to 8.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Non-leveled DDR2 Topology Fails Timing with Stratix V Devices

A non-leveled topology does not work with the DDR2 protocol targeting Stratix V devices.

Affected configurations

This issue affects all DDR2 configurations using a non-leveled topology targeting Stratix V devices.

Design Impact

The design fails to achieve timing targets.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations

Designs containing both UniPHY and ALTMEMPHY instantiations may encounter erroneous clock failures during timing analysis.

Affected configurations

This issue affects all configurations containing both UniPHY and ALTMEMPHY instantiations.

Design Impact

Timing analysis may incorrectly report that some paths are failing timing.

Workaround

The workaround for this issue is to open the UniPHY `<core_name>_report_timing.tcl` and `<core_name>_pin_map.tcl` files in an editor, and make the following change in each file:

Locate the `traverse_to_ddio_out_pll_clock` function name, and append the numeral 2 to the function name, making it `traverse_to_ddio_out_pll_clock2`.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error

Simulation with NC Sim or Riviera-PRO may fail with the error message:
Unsupported memory slice specification using part select or indexed part select.

Affected configurations

This issue affects all configurations using the Nios II-based sequencer.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to open the `sequencer_scc_mgr.sv` file in an editor, and locate the following code:

```
integer unsigned setting_offsets[1:9];
t_setting_mask setting_masks [1:9];

generate
    if (FAMILY == "STRATIXV")
    begin
        assign setting_offsets[1:9] = '{ 'd0, 'd12, 'd17, 'd25, 'd30, 'd36, 'd0,
        'd6, 'd12 };
        assign setting_masks [1:9] = '{ 'b011111111111, 'b011111,
        'b011111111, 'b011111, 'b0111111, 'b0111111, 'b0111111,
        'b011111111111 };
    end
    else
    begin
        assign setting_offsets[1:9] = '{ 'd0, 'd4, 'd8, 'd12, 'd17,
        'd21, 'd0, 'd4, 'd7 };
        assign setting_masks [1:9] = '{ 'b01111, 'b01111, 'b01111,
        'b11111, 'b01111, 'b00111, 'b01111, 'b00111, 'b01111 };
    end
endgenerate
```

For Stratix V devices, replace the preceding code with the following:

```
integer setting_offsets[1:9] = '{ 'd0, 'd12, 'd16, 'd24, 'd27, 'd33, 'd0,
'd6, 'd12 };
t_setting_mask setting_masks [1:9] = '{ 'b011111111111, 'b01111,
'b0111111111, 'b0111, 'b0111111, 'b0111111, 'b0111111,
'b011111111111 };"
```

For non-Stratix V device families, replace the code with the following:

```
integer setting_offsets[1:9] = '{ 'd0, 'd4, 'd8, 'd12, 'd17, 'd21, 'd0,
'd4, 'd7 };
t_setting_mask setting_masks [1:9] = '{ 'b01111, 'b01111, 'b01111, 'b11111,
'b01111, 'b00111, 'b01111, 'b00111, 'b01111 };
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

ECC and CSR Design Fail Timing

ECC and CSR design will fail timing in the Quartus II software.

Affected configurations

This issue affects all configurations with the **Enable Configuration and Status Register Interface** or **Enable Error Detection and Correction Logic** options enabled.

Design Impact

The design will fail timing.

Workaround

The workaround for this issue is as follows:

1. Create a new SDC file in your project.
2. Add the following lines to your SDC file:

```
set_multicycle_path -from [get_keepers {*csr_*}] -to [get_keepers {*}]  
-setup -end 2  
set_multicycle_path -from [get_keepers {*csr_*}] -to [get_keepers {*}]  
-hold -end 2
```
3. Add the SDC file to your project by clicking **Add/Remove Files in Project** from the **Project** menu.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

VHDL-Generated Fileset Can Encounter Synthesis Problems

An error in the VHDL-generated wrapper for the synthesis fileset can result in a variety of synthesis problems.

Affected configurations

This issue affects all configurations using VHDL.

Design Impact

Synthesis problems can result.

Workaround

The workaround for this issue is to open the generated wrapper file in a text editor, and replace all ports of the form `std_logic_vector(0 downto 0)` with `std_logic`.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

UniPHY CSR Ports Not Functioning Correctly

The CSR ports in UniPHY-based interfaces do not function correctly.

Affected configurations

This issue affects all configurations using CSR ports.

Design Impact

The CSR ports do not function correctly.

Workaround

There is no workaround for this issue. Consider using the JTAG Avalon master interface instead.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

User Guide Contains Imprecise Clock Information

The Phase and Clock Network Type columns of tables 6-1 and 6-2 in the user guide contain generalized clock phase and network type information that may not be applicable to your design. In reality, clock phase and network type are dependent on both the target device type and the specific parameterization of your particular IP core.

Affected Configurations

This issue affects all configurations.

Design Impact

This is a documentation issue and has no design impact.

Workaround

The workaround to determine correct clock phase is to run the TimeQuest Timing Analyzer and consult the Clocks Summary report. The workaround to determine clock network type is to consult the Quartus Settings File (.qsf) for your design.

Solution Status

This issue will be fixed in a future version of the External Memory Interface Handbook.

UniPHY IP Generation Fails if Quartus II Path Contains a Space

UniPHY IP generation fails if the installation path of the Quartus II software contains one or more spaces.

Affected configurations

This issue affects all configurations.

Design Impact

UniPHY IP generation fails.

Workaround

The workaround for this issue is to ensure that the Quartus II installation path contains no spaces.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Efficiency Monitor Latency Values Are Incorrect

The Efficiency Monitor and Protocol Checker counts read latencies incorrectly for Avalon burst counts equal to 1; this causes the EMIF Toolkit to report incorrect values for minimum and maximum read latencies.

This issue occurs if you measure efficiency with the example design driver; however, if you use your own custom driver that does not issue an Avalon burst count size equal to 1, the error will not occur.

Affected configurations

This issue affects all configurations with Avalon burst count equal to 1.

Design Impact

Incorrect minimum and maximum read latencies are reported.

Workaround

The workaround for this issue is to use a custom driver that does not issue an Avalon burst count equal to 1.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Memory Controller Uses 1T Memory Timing

The HPC II memory controller now uses 1T memory timing, even in half-rate designs; 1T memory timing can reduce address and command margins, especially for designs targeting DIMMs. You should ensure that your board designs are sufficiently robust to maintain the memory clock rising edge within the 1T address-command window.

You can use the **Additional address and command clock phase** option on the **PHY Settings** tab of the parameter editor to adjust the phase of your address and command if necessary.

Affected configurations

This issue affects all configurations.

Design Impact

You should be aware of this controller behavior.

Workaround

There is no workaround for this issue.

Solution Status

This issue will not be fixed.

Simulation Fails When Enable Auto Error Correction Option Enabled

Designs generated with the **Enable Auto Error Correction** option enabled on the **Controller Settings** tab fail during simulation.

Affected configurations

This issue affects all configurations with the **Enable Auto Error Correction** option enabled.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to add the `CTL_ECC_RMW_ENABLED` parameter in the `dut.v` wrapper file that instantiates the controller wrapper file `alt_mem_if_ddr*_controller_top.sv`, so that `CTL_ECC_RMW_EN` is passed to the controller wrapper.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

ECC and CSR Designs Fail in Simulation or Hardware

Designs generated with the **Enable Error Detection and Correction Logic** or **Enable Configuration and Status Register Interface** options turned on can fail in simulation or in hardware.

Affected configurations

This issue affects all configurations with the **Enable Error Detection and Correction Logic** or **Enable Configuration and Status Register Interface** options turned on.

Design Impact

The design fails in simulation or in hardware.

Workaround

The workaround for this issue is as follows:

1. Open the `<design_name>/submodules/alt_mem_ddrx_csr.v` file in an editor.
2. Make the following changes under Module Parameter Definition:
 - change `BL_BUST_WIDTH = 4` to `BL_BUST_WIDTH = 5`
 - change `MEM_IF_CSR_COL_WIDTH = 4` to `MEM_IF_CSR_COL_WIDTH = 5`
 - change `MEM_IF_CSR_BANK_WIDTH = 2` to `MEM_IF_CSR_BANK_WIDTH = 3`
 - change `MEM_IF_CSR_CS_WIDTH = 2` to `MEM_IF_CSR_CS_WIDTH = 3`
3. At approximately line 1040, change the line:

```
assign cfg_burst_length = csr_bl [BL_BUS_WIDTH - 1 : 0];
```

to

```
assign cfg_burst_length = {(BL_BUS_WIDTH - 4){1'b0}}, csr_bl};
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Example Project Fails to Simulate When HardCopy Compatibility Enabled

The example project for designs generated with **HardCopy Compatibility Mode** enabled can fail to simulate.

Affected configurations

This issue affects DDR2 and DDR3 UniPHY designs generated with **HardCopy Compatibility Mode** enabled.

Design Impact

The example project fails in simulation.

Workaround

The workaround for this issue is to modify two files, as follows:

1. In a text editor, open the file
`<variant_name>_example_design/simulation/<variant_name>_example_sim/
submodules/<variant_name>_example_sim_<variant_name>_example_sim.v`
2. In the above file, change the line
`.INIT_FILE = ("dut_dut_e0_if0_p0_sequencer_rom.v")`
to
`.INIT_FILE =
("<variant_name>_example_sim_<variant_name>_example_sim_e0_if0_p0_
sequencer_rom.v")`
3. In a text editor, open the file
`<variant_name>_example_design/simulation/<variant_name>_example_sim.qsf`
4. In the above file, add the following lines:
`set_global_assignment -name EDA_TEST_BENCH_FILE
<variant_name>_example_sim/submodules/hc_rom_reconfig_gen.sv -
section_id uniphy_rtl_simulation -hdl_version SystemVerilog_2005`

and

`set_global_assignment -name SOURCE_FILE
<variant_name>_example_sim/submodules/<variant_name>_example_sim_
<variant_name>_example_sim_e0_if0_p0_sequencer_rom.hex`

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

NativeLink RTL Simulation May Fail

NativeLink RTL simulation may fail and report warnings that a file could not be opened for reading.

Affected configurations

This issue affects all UniPHY protocols.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to edit the project's **.qsf** settings file and add to it all the **.hex** and **.mif** files residing in the directory:

```
<variant_name>_example_design/simulation/<variant_name>_example_sim/  
submodules/
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Simulation Fails for Memory Additive CAS Latency Settings > 0

The **Memory Parameters** tab in the parameter editor allows you to set **Memory additive CAS latency** to a value greater than zero; however, if you chose a value greater than zero, the design will fail in simulation.

Affected configurations

This issue affects designs using the high-performance controller II (HPC II), with **Memory additive CAS latency** set to a value greater than zero.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to add the `MEM_ADD_LAT` parameter to the `dut.v` wrapper file that instantiates the controller wrapper (`alt_mem_if_ddr*_controller_top.sv`), so that `MEM_ADDLAT` is passed down to the controller wrapper.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Error Messages in ModelSim Flow for Eclipse

Designs generated with the **Enable support for Nios II ModelSim flow in Eclipse** option enabled can produce error messages reporting attempts to read from uninitialized data locations.

Affected configurations

This issue affects DDR2 and DDR3 designs generated with the **Enable support for Nios II ModelSim flow in Eclipse** option enabled.

Design Impact

Error messages are displayed.

Workaround

There is no workaround for this issue; you may ignore the error messages.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Unable to Directly Recompile 10.1 Design in 11.0

A design compiled in the Quartus II software version 10.1 cannot be directly recompiled in version 11.0, for speeds greater than 500 MHz.

Affected configurations

This issue affects designs targeting Stratix V devices at speeds greater than 500 MHz.

Design Impact

The 10.1 design cannot be directly recompiled in 11.0.

Workaround

The workaround for this issue is to load the `<variation_name>.v` file generated by the version 10.1 MegaWizard Plug-In Manager into the version 11.0 MegaWizard Plug-In Manager and regenerate the IP core in version 11.0.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Multi-cast Write Control Not Supported

If you enable the **Multi-cast write control** option, the design will fail in simulation.

Affected configurations

This issue affects designs using the high-performance controller II (HPC II), with the **Multi-cast write control** option turned on.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to add the `MULTICAST_WR_EN` parameter to the `dut.v` wrapper file that instantiates the controller wrapper (`alt_mem_if_ddr*_controller_top.sv`), so that `MULTICAST_WR_EN` is passed down to the controller wrapper.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

ModelSim Waveform Viewer Shows Only clk and reset Signals

ModelSim simulation of the example design for MegaWizard-generated systems displays only the clk and reset signals in the waveform viewer.

Affected configurations

This issue affects all MegaWizard-generated DDR2 and DDR3 SDRAM Controller with UniPHY interfaces.

Design Impact

Only clk and reset waveforms are displayed.

Workaround

The workaround for this issue is as follows:

1. Open the existing
`<variant_name>_example_design/simulation/<variant_name>_example_sim.qsf`
file in a text editor and add the following line to the file:

```
set_global_assignment -name EDA_NATIVELINK_SIMULATION_SETUP_SCRIPT  
my_wave.do -section_id eda_simulation
```

Where `<my_wave>.do` is a file name of your choice.

2. Create a ModelSim `<my_wave>.do` file in the
`<variant_name>_example_design/simulation` directory.

Ensure that the `<my_wave>.do` file has the following content:

```
"  
add wave dut/<variant_name>_example_sim_inst/*  
run -all  
"
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

PLL Master Required for Simulation of PLL Slave

The example simulation design (generated in the
`<variation_name>_example_design\simulation` folder) does not function correctly if the core is parameterized with **PLL Sharing Mode = Slave**, **DLL Sharing Mode = Slave**, or **OCT Sharing Mode = Slave**.

Affected configurations

This issue affects all protocols with UniPHY interfaces employing slave PLLs, DLLs, or OCTs.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to ensure that a master instantiation is provided to drive the slave. To do this, follow these steps (a PLL example is shown):

1. Generate a second, identically parameterized, IP core with **PLL Sharing Mode** set to **Master**.
2. Manually instantiate the second IP core in the top-level file of the slave core's example design,

```
<variation_name>_example_design\simulation\  
<variation_name>_example_sim.v.
```

3. Connect the master and slave by following the usual PLL sharing flow.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Minimum Pulse Width Timing Failure

Designs targeting Stratix V devices at speeds greater than 500MHz might experience minimum pulse width timing failure.

Affected Configurations

This issue affects designs targeting Stratix V devices at speeds greater than 500MHz.

Design Impact

The issue manifests as a minimum pulse width timing failure.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Efficiency Monitor Statistics Incorrect for Initial Sample

The initial statistics produced by the Efficiency Monitor are likely to be incorrect while the interface is calibrating.

Affected configurations

This issue affects DDR2 and DDR3 UniPHY designs.

Design Impact

The initial data produced by the Efficiency Monitor may be incorrect.

Workaround

The workaround for this issue is to wait for calibration to finish before rereading the statistics from the Efficiency Monitor.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Simulation Fails with “Undefined System Task Call” Error

An issue with the JTAG Avalon master can cause simulation to fail with the following error message:

```
Error-[UST] Undefined System Task Call
submodules/altera_pli_streaming.v, 53
Undefined System Task call to '$do_transaction'.
```

Affected configurations

This issue affects all UniPHY-based external memory interfaces that use the internally instantiated JTAG Avalon master for the CSR port or the Efficiency Monitor and Protocol Checker.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to remove the `altera_pli_streaming` file from the list of files used in the simulation if the programming language interface (PLI) is turned off.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Using UniPHY-based Memory IP with SOPC Builder

A workaround is necessary to enable UniPHY-based memory IP support with SOPC Builder.

Affected Configurations

This issue affects all UniPHY-based designs with SOPC Builder.

Design Impact

The workaround is necessary or else the design fails.

Workaround

Perform the following steps to enable UniPHY-based memory IP support in SOPC Builder:

1. On the **Controller Settings** tab in the DDR2 and DDR3 SDRAM Controller with UniPHY parameter editor, turn on **Generate power-of-2 data bus widths for SOPC Builder**.
2. On the **Controller Settings** tab in the DDR2 and DDR3 SDRAM Controller with UniPHY parameter editor, turn on **Generate SOPC Builder compatible resets**.
3. After generating your external memory interface IP system, open your **.sopc** file in a text editor. In the **.sopc** file, locate lines similar to the following (where *<instance_name>* is the instance name of your IP core):

```
//reset sources mux, which is an e_mux
assign reset_n_sources = ~(~reset_n |
0 |
0 |
~<instance_name>_avl_resetrequest_n_from_sa |
~<instance_name>_avl_resetrequest_n_from_sa);
```

Replace each occurrence of *~<instance_name>_avl_resetrequest_n_from_sa* with 0 (zero), so that the above snippet becomes as follows:

```
//reset sources mux, which is an e_mux
assign reset_n_sources = ~(~reset_n |
0 |
0 |
0 |
0);
```

4. Manually reconnect the UniPHY reset inputs (*global_reset_n* and *soft_reset_n*) in the SOPC Builder-generated top-level file (*system.v*), as follows:

```
.global_reset_n (reset_n_sources),
.soft_reset_n (reset_n_sources),
```

Solution Status

This issue will not be fixed.

Using Avalon-MM Traffic Generator and BIST Engine

A workaround is necessary to enable the Avalon-MM Traffic Generator and BIST Engine.

Affected Configurations

This issue affects all UniPHY-based configurations using the Avalon-MM Traffic Generator and BIST Engine.

Design Impact

The workaround is necessary or else the Avalon-MM Traffic Generator and BIST Engine fails.

Workaround

Perform the following steps to enable the workaround:

1. On the **Controller Settings** tab in the DDR2 and DDR3 SDRAM Controller with UniPHY parameter editor, turn on **Generate power-of-2 data bus widths for SOPC Builder**.
2. On the **Controller Settings** tab in the DDR2 and DDR3 SDRAM Controller with UniPHY parameter editor, turn on **Generate SOPC Builder compatible results**.
3. Manually reconnect the reset input (reset_n) in the top-level file (system.v), as follows:

```
.reset_n (reset_n_sources),
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Fitter Error When Compiling DDR2 Designs Below 240MHz

For DDR2 designs operating at frequencies of 240MHz or less, the Fitter might display the error message: Can't place Top/Bottom or Left/Right PLL.

Affected configurations

This issue affects designs targeting DDR2 memory devices at memory frequencies of 240MHz or less.

Design Impact

The Fitter fails to fit the design.

Workaround

The workaround for this issue is to turn on the **Remove Duplicate Registers** synthesis option.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Simulation Fails when Generating VHDL for Designs Using Nios II-based Sequencer

For designs using the Nios II-based sequencer, simulation can fail when generating VHDL output.

Affected configurations

This issue affects designs using the Nios II-based sequencer and VHDL.

Design Impact

Simulation fails.

Workaround

The workaround for this issue requires that you manually modify certain files.

1. Look for three **.vhd** files with file names beginning with a string similar to the following:

```
dut_dut_e0_if0_p0_qsys_sequencer_cpu_inst_jtag_debug_module
```

where *<dut>* is the name that you have specified for your project.

2. Open each of the three files in a text editor and add the following two lines to the beginning of each file:

```
library altera_mf;  
use altera_mf.altera_mf_components.all;
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys

The alt_mem_if interface supports the sharing of PLLs, DLLs, and OCTs using a sharing conduit; however, the conduit supports only point-to-point connections in Qsys, and therefore cannot be used to share a single master with multiple slaves.

Affected configurations

This limitation affects UniPHY-based designs built using Qsys.

Design Impact

The sharing of a single master with multiple slaves is not supported.

Workaround

There is no workaround for this limitation.

Solution Status

This issue will not be fixed.

Conduit Error Messages Displayed in Qsys

When generating a UniPHY-based IP core in Qsys, warning messages may appear stating that a given signal must be connected to a conduit. You may ignore such messages.

Affected configurations

This issue affects UniPHY-based designs generated with Qsys.

Design Impact

This issue has no design impact.

Workaround

Ignore the warning messages stating that a given signal must be connected to a conduit.

Solution Status

This issue will not be fixed.

DDR3 ODT Fails in Simulation with Denali

DDR3 ODT failures can occur in simulation with Denali.

Affected configurations

This issue affects DDR3 configurations with unbuffered DIMM, multiple DIMMs, ODT enabled, and a number of slots greater than 1.

Design Impact

This issue can result in a simulation error, and can also result in data corruption in hardware.

Workaround

There are two possible workarounds for this issue:

Option 1: Open the `alt_mem_ddrx_controller_st_top.v` file and add 1 (clk) to the equation used to derive the localparams `CFG_EXTRA_CTL_CLK_RD_TO_WR_DIFF_CHIP` and `CFG_EXTRA_CTL_CLK_WR_TO_RD_DIFF_CHIP`.

Option 2: Open the generated file `<variation_name>_alt_mem_ddrx_controller_top.v` and change the localparam `CFG_READ_ODT_CHIP` value to `'h0`.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

EMIF Toolkit Reports Incorrect CAS Latency for 10.1 IP Opened in 11.0

If you open an IP core generated in version 10.1 of the Quartus II software in version 11.0 of the EMIF Toolkit, the toolkit reports an incorrect CAS latency value.

Affected configurations

This issue affects all IP cores generated in version 10.1 of the Quartus II software and opened in version 11.0 of the EMIF Toolkit.

Design Impact

The reported CAS latency is incorrect.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Example Design Simulation May Fail in NC Sim

The autogenerated example design can fail during simulation in NC Sim.

Affected configurations

This issue affects all configurations.

Design Impact

This issue can cause the autogenerated example design to fail during simulation in NC Sim.

Workaround

Do not attempt to simulate the autogenerated example design in NC Sim.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Must Enable Support for Nios II ModelSim Flow in GUI

If you intend to use your generated IP with the **Run as Nios II ModelSim flow** in Eclipse, you must turn on the **Enable support for Nios II ModelSim flow in Eclipse** option on the **Diagnostics** tab in the parameter editor, or else your design may fail in Eclipse.

Affected configurations

This issue affects all designs targeting the ModelSim flow.

Design Impact

This issue can cause your design to fail in Eclipse.

Workaround

Ensure that you turn on the **Enable support for Nios II ModelSim flow in Eclipse** option on the **Diagnostics** tab in the parameter editor.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Example Design Can Fail For Certain Parameterizations

The autogenerated example design can fail for parameterizations with `byteenables` (data mask) disabled and burst length greater than the rate ratio.

Affected configurations

This issue affects UniPHY-based designs generated with `byteenables` (data mask) disabled and burst length greater than the rate ratio.

Design Impact

This issue causes the example design to fail.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Example Design Without DM Pins Enabled Will Fail

Any generated example design that does not have DM pins enabled will fail in simulation and in hardware.

Affected configurations

This issue affects any example design that does not have DM pins enabled.

Design Impact

The design will fail in simulation and will not work in hardware.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Simulation of Example Designs Can Fail or Produce Warnings

The example design for simulation may fail to compile or trigger compiler warnings in either the VCS or NC Sim simulators, if the simulation scripts are generated from NativeLink.

Affected Configurations

This issue affects all simulations of the generated example design.

Design Impact

Simulation in NC Sim or VCS may fail; other simulators may issue warning messages.

Workaround

The following workarounds apply to this issue:

- For simulation in VCS, add the `-debug_pp` option to the `.vcs` file generated by NativeLink.
- For simulation in NC Sim or any other simulator, remove the `$vcdpluson;` line from the `<variation_name>_example_design/simulation/<variation_name>_example_sim/submodules/status_checker.sv` file.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Compilation of a UniPHY Example Design Can Produce Warnings

If you compile a UniPHY-based example design in the Quartus II software, TimeQuest may produce warning messages similar to the following:

```
Warning: Ignored filter at altera_reset_controller.sdc (17):
*|alt_rst_sync_up1|altera_rest_synchronizer_int_chain*|aclr could not
be matched with a pin
Warning: Ignored set_false_path at altera_reset_controller.sdc (17):
Argument <from> is an empty collection
```

Affected Configurations

This issue affects all UniPHY-based example designs.

Design Impact

Warning messages are displayed.

Workaround

You may safely ignore these warning messages. To prevent these warning messages from appearing, you can modify the Qsys-generated Synopsys Design Constraints file `altera_reset_controller.sdc` so that the paths mentioned in the warnings conform to the specific hierarchy of your design. (Be aware that any changes that you make to the `.sdc` file might be overwritten if you regenerate your IP core.)

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Error in Graphical Display of DQ Calibration Margin in EMIF Toolkit

The right-hand side of the Read Data Valid Windows and Write Data Valid Windows display in the External Memory Interface Toolkit displays one too many green boxes in each row.

Affected configurations

This issue affects all configurations.

Design Impact

Information displayed in the Read Data Valid Windows and Write Data Valid Windows is inaccurate.

Workaround

Margin values reported in the Margining Status Report are correct. Rely on the values in the Margining Status Report rather than the graphical representations of the Read Data Valid Windows and Write Data Valid Windows.

Solution Status

This issue will be fixed in a future version of the EMIF Toolkit.

NativeLink Simulation fails for VHDL Output

When you specify VHDL output for the DDR2 and DDR3 SDRAM Controller with UniPHY and attempt to simulate using NativeLink, NativeLink fails and reports that it cannot find the file `<design_name>.vho` in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

This workaround for this issue is to not use NativeLink for simulations of VHDL designs, but to set up simulation manually instead.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.0 of the Quartus II software, when a user specifies VHDL output for the DDR2 and DDR3 SDRAM Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file `<design_name>.vho` in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

This workaround for this issue is to edit the `<design_name>.vhd` file and remove the line similar to the following:

```
-- IPFS_FILES : <design_name>.vho
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Timing-related Warning Messages When Sharing PLLs on Stratix V Devices

When instantiating a design in PLL/DLL slave mode on a Stratix V device, the TimeQuest Timing Analyzer may display warning messages similar to the following:

```
Warning: Ignored filter at slave_report_timing_core.tcl(176):  
slave_inst0|controller_phy_inst|memphy_top_inst|umemphy|uio_pads|  
dq_ddio[1].ubidir_dq_dqs|altdq_dqs2_inst|thechain|clkin could not be  
matched with a keeper or register or port or pin or cell or net  
  
Warning: Command get_path failed
```

Affected Configurations

This issue affects Stratix V designs instantiated in PLL/DLL slave mode.

Design Impact

The resulting timing analysis is incorrect.

Workaround

This issue has no workaround. The warning messages can be safely ignored; however, do not rely on the accuracy of the resulting timing analysis.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Devices Faster than 533MHz Require Manual Derating

The DDR3 SDRAM Controller with UniPHY provides automatic derating based on the AC175 threshold. Memory devices faster than 533 MHz require derating based on the AC150 threshold.

Affected configurations

This issue affects all configurations using memory devices faster than 533 MHz.

Design Impact

This issue can result in inaccurate timing analysis.

Workaround

You should calculate derated setup and hold values for your memory device, and enter those values in the DDR3 SDRAM Controller with UniPHY parameter editor.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Reset Synchronizer May Cause Design to Fail Timing

Systems generated with SOPC Builder or Qsys may fail timing closure due to paths that include a reset synchronizer.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails timing closure.

Workaround

A workaround for this issue is to apply the following constraint in the TimeQuest Timing Analyzer:

For SOPC Builder:

```
set_false_path -from {dut_sopc_top_reset_clk_0_domain_synch_module:  
dut_sopc_top_reset_clk_0_domain_synch*}
```

For Qsys:

```
set_false_path -from *:rst_controller*|*:alt_rst_sync_uq1|  
altera_reset_synchronizer_int_chain[*] -to *:controller_phy_inst|  
*:memphy_top_inst|*:umemphy|*:ureset|*:ureset_*_clk|reset_reg[*]
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Compilation Fails if Synthesis Fileset is Mixed with Example Project Files

Compilation fails if the **Files** list in the **Settings** dialog box in the Quartus II software includes files from both the example project located at `<working_dir>/<variation_name>_example_design_fileset/example_project/` and the synthesis fileset located at `<working_dir>/<variation_name>`.

Affected Configurations

This issue affects all configurations.

Design Impact

Compilation fails.

Workaround

A workaround for this issue is to perform the following steps:

1. In an editor, open the `<variation_name>_driver.sv` file, located in the `<working_dir>/<variation_name>_example_design_fileset/example_project/` directory.
2. In the `<variation_name>_driver.sv` file, change the entity name `<variation_name>_reset_sync` to `<variation_name>_<num>_reset_sync`, where *num* is the same value as in the `<variation_name>_<num>_reset_sync.v` filename in the `<working_dir>/<variation_name>/` directory.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Warning Messages Displayed When Compiling for Stratix V Devices

When compiling a design for Stratix V devices, the system may display numerous PLL-related warning messages similar to the following:

```
Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 do not have a PLL
clock to compensate specified - the Fitter will attempt to compensate all
PLL
```

```
Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 use multiple
different clock network types - the PLL will compensate for output clocks
```

```
Warning: PLL cross checking found inconsistent PLL clock settings:
```

```
Warning: Node: mem_if|controller_phy_inst|memphy_top_inst|
pll1~FRACTIONAL_PLL|mcntout was found missing 1 generated clock that
corresponds to a base clock with a period of: 8.000
```

```
Warning: Clock: mem_if|ddr3_pll_write_clk was found on node:
mem_if|controller_phy_inst|memphy_top_inst|pll3|outclk with settings that
do not match the following PLL specifications:
```

```
Warning: -multiply_by (expected: 21, found: 4264000)
```

```
Warning: -divide_by (expected: 5, found: 1000000)
```

Warning: -phase (expected: 0.00, found: 90.00)

These warning messages are expected and can be ignored.

Affected Configurations

This issue affects all configurations targeting Stratix V devices.

Design Impact

This issue has no design impact.

Workaround

There is no workaround for this issue. You can safely ignore the error messages.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Cannot Launch MegaWizard Plug-In Manager by Opening Example Design

You cannot reopen your project in the MegaWizard Plug-In Manager by clicking on your generated IP instantiation

`<working_dir>/<variation_name>_example_design/example_project/`

`<variation_name>_example/<variation_name>_example.v`

or

`<working_dir>/<variation_name>_example_design/simulation/<variation_name>_`

`example_sim/<variation_name>_example_sim.v`

Affected configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

To reopen your variation in the MegaWizard Plug-In Manager, follow these steps:

1. In the Quartus II software, click **MegaWizard Plug-In Manager** on the **Tools** menu.
2. Click **Edit an existing custom megafunction variation** and specify:
`<working_dir>/<variation_name>.v`.

Solution Status

This issue will not be fixed.

Example Design May Not Compile for IP Cores from Earlier Versions

The example design provided with version 10.1 may not compile with IP cores migrated from earlier versions of the Quartus II software.

Affected configurations

This issue affects all configurations.

Design Impact

Attempting to compile the example design with IP cores migrated from earlier versions of the Quartus II software may fail with the following message:

```
Error:instance "ureset_driver_clk" instantiates undefined entity  
"<variation_name>_reset_sync"
```

Workaround

The workaround for this issue is to perform the following steps:

1. In the Quartus II software, open the **Settings** dialog box on the **Assignments** menu.
2. In the **Category** tree of the **Settings** dialog box, click **Files** to display the files list.
3. Remove all the UniPHY files, including the **.qip** file and example project files, from the migrated project assignments.
4. Add to the project the newly generated **.qip** file located in the `<working_dir>/<variation_name>_example_design_fileset` directory.
5. Add to the project all of the files except for the memory model, from the directory `<working_dir>/<variation_name>_example_design_fileset/example_project`.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

SOPC Builder-generated Systems Cannot Serve as Top-Level Design

Systems generated with SOPC Builder cannot serve as the top-level design, because SOPC Builder automatically exports the `parallelterminationcontrol` and `seriesterminationcontrol` OCT control signals as top-level ports, but these signals must not be exposed at the top level.

Affected configurations

This issue affects all configurations generated with SOPC Builder.

Design Impact

Compilation fails.

Workaround

Perform either of the following procedures to work around this issue:

- Create a top-level wrapper which instantiates the SOPC Builder-generated system, and does not make any connection to the `parallelterminationcontrol` or `seriesterminationcontrol` signals.

or

- Open the top-level SOPC Builder system file (for example, *system.v*), and delete the wire names from within the brackets for the `parallelterminationcontrol` and `seriesterminationcontrol` signals for all UniPHY cores. The resulting lines should appear as follows:

```
.parallelterminationcontrol ()  
.seriesterminationcontrol ()
```

The wire names that you delete from within the brackets must also be removed from all other locations in the top-level system file, including the top-level port list.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices

In Stratix V devices, the corner I/O banks are expected to have higher core-to-I/O and I/O-to-core delay and skew values than the other I/O banks, and are unsuitable for interfacing with external memory at frequencies above 667 MHz.

The characteristics of the corner I/O banks are not yet reflected in the Stratix V timing models available in version 10.1 of the Quartus II software; consequently, timing analysis will not accurately characterize the performance of the corner I/Os.

Affected Configurations

This issue affects all configurations targeting Stratix V devices at frequencies above 667 MHz.

Design Impact

This issue can adversely affect timing.

Workaround

Avoid using the outer I/O banks at the upper and lower sides of the device.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Incorrect Clock Uncertainty

A clock uncertainty related to the read FIFO buffer clocked by DQS can result in inaccurate setup and hold slack values.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can cause setup and hold slack values to be inaccurate.

Workaround

The workaround for this issue is to manually edit the PHY .sdc file located in the `<variation_name>/constraints/` directory, and add the following two lines to the Multicycle Constraints section of the file:

```
set_max_delay -from *ddio_in_inst_regout* -0.05
set_min_delay -from *ddio_in_inst_regout* [expr -$t(CK) + 0.05]
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

User Guide Contains Incorrect Clock Information

In the user guide, table 6-1 contains incorrect clock phase information for `pll_mem_clk` and `pll_write_clk`.

Also, table 6-2 is inapplicable and should be ignored.

Affected Configurations

This issue affects all configurations.

Design Impact

This is a documentation issue and has no design impact.

Workaround

The correct phase for `pll_mem_clk` is 0° for interfaces with the Leveling Interface Mode set to **Leveling**, and -45° for interfaces with Leveling Interface Mode set to **Non-leveling**.

The correct phase for `pll_write_clk` is 90° for interfaces with the Leveling Interface Mode set to **Leveling**, and -135° for interfaces with Leveling Interface Mode set to **Non-leveling**.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Using Burst Merging Feature

The burst merging feature is turned off by default when you generate a controller. If your traffic exercises patterns that you can merge, you should turn on merging. Turning merging on may affect f_{MAX} performance.

Affected Configurations

This issue affects all designs.

Design Impact

There is a performance improvement if you can merge traffic when you turn on this feature.

Workaround

To work around this issue, turn on merging, by changing the `ENABLE_BURST_MERGE` parameter from 0 to 1 in the `<variation>.v` file.

Solution Status

This issue will never be fixed.

Autoprecharge Feature is Not Available

You can select autoprecharge in the MegaWizard interface and the *DDR2 and DDR3 SDRAM Controller with UniPHY IP User Guide v10.0* documents autoprecharge, but the feature is not enabled.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue affects all designs.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Global Signal Assignments Not Applied

The Fitter sometimes does not honor GLOBAL signal assignments applied by the `<variation name>_pin_assignments.tcl` script.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no impact on the design, but can result in suboptimal resource placement and can contribute to difficulties in achieving timing closure.

Workaround

To determine whether the Quartus II software properly applies GLOBAL assignments, check the Fitter Report and verify whether any GLOBAL signal assignment referring to a PLL output port (for example, `... |auto_generated|clk[*]`) appear in the Ignored Assignments section.

If there is a GLOBAL assignment to a PLL output port listed in Ignored Assignments, you can correct the problem by running Analysis and Synthesis and then running the Fitter. You should then verify in the Fitter Report that the assignment is no longer ignored.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

BSF File Not Generated

The IP core does not generate a `.bsf` file, and therefore is not compatible with workflows requiring a `.bsf` file.

Affected Configurations

This issue affects all configurations.

Design Impact

Errors are likely to occur with workflows using the Schematic Editor or Symbol Editor.

Workaround

Do not use the Schematic Editor or the Symbol Editor with the IP core.

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Selecting VHDL Gives a Verilog HDL IP Core

If you select VHDL in the MegaWizard interface and generate a DDR2 or DDR3 SDRAM controller with UniPHY IP core, the generated core is in Verilog HDL.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The issue affects all VHDL designs.

Workaround

To generate a VHDL IP core follow these steps:

1. In a text editor open
`<Quartus II directory>\ip\altera\uniphy\lib\common_ddrx.tcl.`
2. Search for the string "LANGUAGE" that appears in the following code:

```
append param_str ",LANGUAGE=[get_generation_property HDL_LANGUAGE]"
```
3. Change this line to the following code:

```
append param_str ",LANGUAGE=vhdl"
```
4. Continue searching for the next occurrence of the string "LANGUAGE" which appears in the following code:

```
if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
    add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
    puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \${::quartus(qip_path) ${outputname}.v\]"
} else {
    add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
    puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\${::quartus(qip_path) ${outputname}.vhd\]"
}
}
```
5. Comment out the if line, the else line, and the block of code in the conditional section so that the code in the "else" block always executes, similar to the following code:

```
# if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
#     add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
#     puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \${::quartus(qip_path) ${outputname}.v\]"
# } else {
    add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
    puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\${::quartus(qip_path) ${outputname}.vhd\]"
# }
```
6. Use the MegaWizard interface to generate a UniPHY-based IP core.



To generate a Verilog HDL IP core, restore the original **common_ddrx.tcl** file.

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Designs Without Leveling Fail in Stratix V Devices

If you target Stratix V devices with a IP core without leveling, the design fails.

Affected Configurations

This issue affects all Stratix V designs.

Design Impact

Compilation fails.

Workaround

To work around this issue, disable the DM pins.



The MegaWizard interface does not support design without leveling targeting Stratix V devices (the option is disabled), but you can generate a Stratix V design with leveling.

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Quartus II Software Cannot Read .mif File for PLL

The Quartus II software gives a warning that it cannot read the .mif file, which causes the PLL to load with unexpected initial settings.

Affected Configurations

This issue affects all designs when you turn on **HardCopy Compatability Mode**.

Design Impact

Compilation fails.

Workaround

To work around this issue, copy the .mif file from the *<variation name>/rtl* directory to the project directory.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Example Design Fails as a Slave

In slave mode, the MegaWizard interface instantiates the PLL in the **example_top.v** file. However for DDR2 and DDR3 SDRAM example designs, the wizard fails to connect the DQS enable clock to the PLL.

Affected Configurations

This issue affects example designs with a slave interface.

Design Impact

This issue has no design impact.

Workaround

To work around this issue, modify **example_top.v** to connect the DQS enable clock (pll_dqs_ena_clk) to the c4 port of the PLL:

```
pll_memphy upll_memphy(
    .areset                (~global_reset_n),
    .inclnk0               (pll_ref_clk),
    .c0                    (pll_afi_clk),
    .c1                    (pll_mem_clk),
    .c2                    (pll_write_clk),
    .c3                    (pll_addr_cmd_clk),
    .c4                    (pll_dqs_ena_clk),
    .c5                    (pll_avl_clk),
    .c6                    (pll_config_clk),
    .locked                (pll_locked)
);
```

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Simulation Fails in Riviera

Simulations with the Riviera software fail.

Affected Configurations

This issue affects all designs.

Design Impact

This issue has no design impact.

Workaround

To work around this issue, modify the following lines in `rand_burstcount_gen.sv` outside of the generate block:

```
localparam MIN_EXPONENT= ceil_log2(MIN_BURSTCOUNT);  
localparam MAX_EXPONENT= log2(MAX_BURSTCOUNT);  
localparam EXPONENT_WIDTH= ceil_log2(MAX_EXPONENT);
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Simulation Fails—PLL Clocks Out of Synchronization

During simulation, the PLL clocks lose synchronization.

Affected Configurations

This issue affects all designs.

Design Impact

This issue causes simulation failures.

Workaround

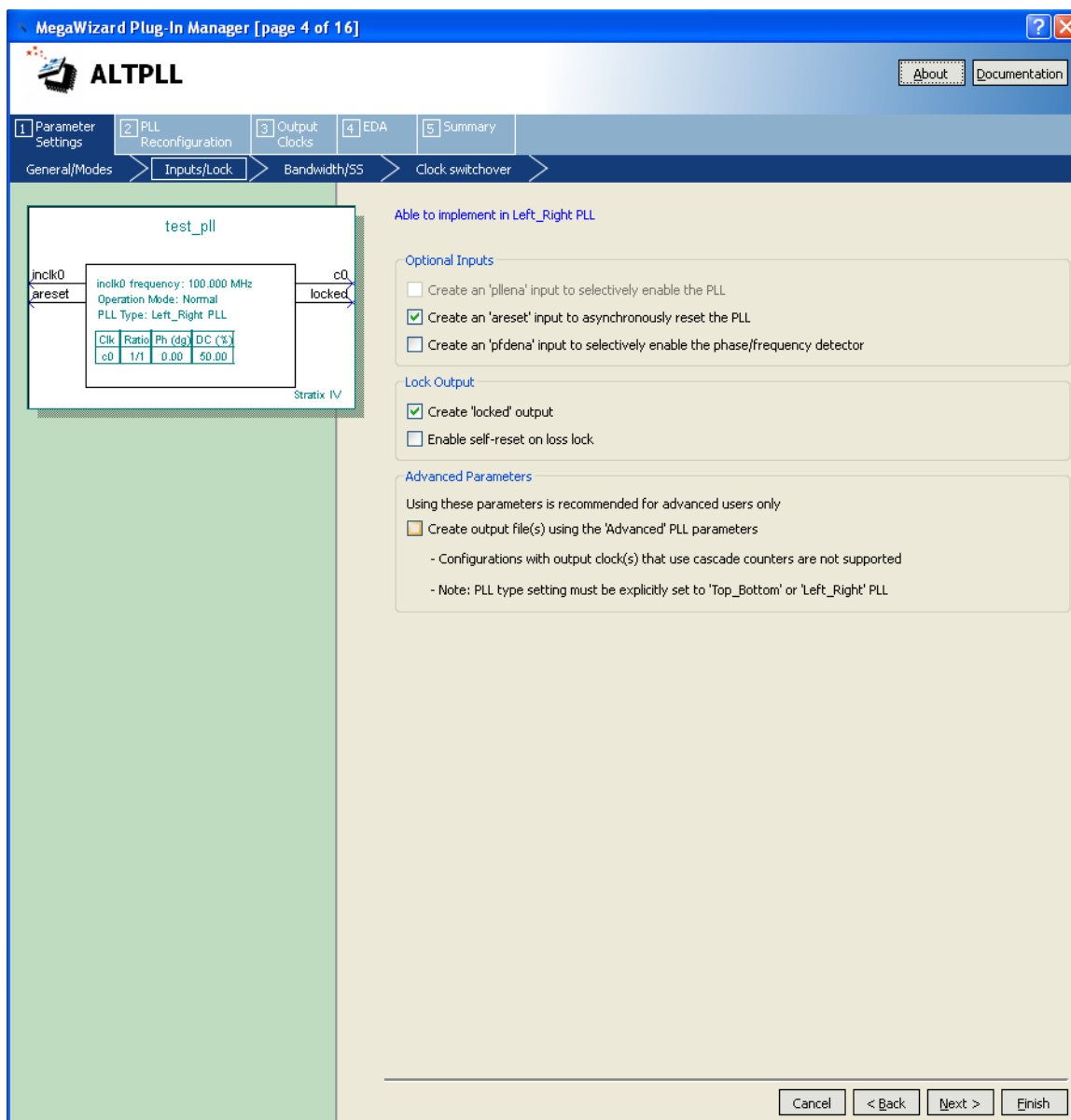
To work around this issue, follow these steps:

1. In text editor open the design file and remove the following line:

```
coverage exclude_file
```

2. In the ALTPLL MegaWizard interface, turn on **Create output files using the Advanced PLL parameters** and regenerate the PLL ().

Figure 10-1. PLL Parameter



Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

SOPC Builder Designs Suffer Low Efficiency

If you use SOPC Builder to instantiate a DDR2 or DDR3 SDRAM Controller with UniPHY IP core, you may find your design has low memory efficiency.

Affected Configurations

This issue affects all designs when you use SOPC Builder to instantiate a DDR2 or DDR3 SDRAM Controller with UniPHY IP core.

Design Impact

The design has low memory efficiency.

Workaround

To work around this issue, use the MegaWizard Plug-In flow to instantiate a DDR2 or DDR3 SDRAM Controller with UniPHY IP core.

Solution Status

This issue is fixed in version 10.0SP1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Revision History

Table 11–1 shows the revision history for the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function.



For more information about the new features, refer to the *DDR3 SDRAM Controller with ALTMEMPHY IP User Guide*.

Table 11–1. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Revision History

Version	Date	Description
11.0 SP1	July 2011	Maintenance release
11.0	May 2011	Added new controller features, including data-reordering capability
10.1	December 2010	Maintenance release
10.0	July 2010	<ul style="list-style-type: none"> Added information for new GUI parameters: Controller latency, Enable reduced bank tracking for area optimization, and Number of banks to track. Removed information about IP Advisor. This feature is removed from the DDR3 SDRAM IP support for version 10.0.

Errata

Table 11–2 shows the issues that affect the DDR3 SDRAM Controller with ALTMEMPHY IP v11.0, 10.1, and 10.0.

Table 11–2. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		11.0 SP1	11.0	10.1	10.0
1 Jul 11	ECC Interrupt Function Not On by Default	✓	✓	—	—
	ECC Registers Not Accessible from Controller Register Map	✓	✓	—	—
	Error Related to Incorrect Syntax of Type Conversion	✓	✓	—	—
	VCS Simulation Fails and Reports that Module was Previously Declared	✓	✓	—	—
	Half Rate Bridge Not Supported	✓	✓	—	—
	System Timestamp Mismatch Warning Message	✓	✓	—	—
	VHDL Example Driver Fails in Simulation	✓	✓	—	—
	DDR3 ODT Fails in Simulation with Denali	Fixed	✓	—	—
15 Dec 10	Resynchronization Registers Incorrectly Placed in Core instead of I/O	—	Fixed	✓	—
	Devices Faster than 533MHz Require Manual Derating	—	Fixed	✓	—
	pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems	✓	✓	✓	—
	Warning Messages Reporting Ignored SDC Constraints	✓	✓	✓	—

Table 11–2. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		11.0 SP1	11.0	10.1	10.0
15 July 10	Error in Board Settings GUI	✓	✓	✓	✓
	Using Merging Feature	✓	✓	✓	✓
	Memory Controller Returns Wrong Data	✓	✓	✓	✓
	Refresh to Precharge Command Timing Violation	✓	✓	✓	✓
	Power-Down Entry Command Timing Violation	✓	✓	✓	✓
	Failure to Regenerate 9.0 Designs in Silent Mode	✓	✓	✓	✓
01 Apr 10	CSR Address 0x005 and 0x006 Contents Cannot be Accessed	✓	✓	✓	✓
	Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate	✓	✓	✓	✓
	Half-Rate Clock Not Connected When Clock Sharing is Enabled	✓	✓	✓	✓
15 Nov 09	Generate Simulation Model Option Gets Disabled	✓	✓	✓	✓
	Designs with Eight Chip Selects Fail Compilation	✓	✓	✓	✓
01 Jul 09	Address Mirroring Not Supported By Memory Simulation Model	✓	✓	✓	✓
15 Mar 09	Memory Preset Parameters Do Not Get Updated	✓	✓	✓	✓
	Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	✓	✓	✓	✓

ECC Interrupt Function Not On by Default

When you turn on the **Enable Error Detection and Correction Logic** option, the ECC Interrupt function is not turned on by default.

Affected configurations

This issue affects all configurations using the 11.0 version of the high-performance controller II.

Design Impact

When a single-bit or double-bit error occurs, the ECC logic does not trigger the `ecc_interrupt` signal.

Workaround

There is no workaround for this issue for VHDL designs.

For Verilog designs, the workaround is to open the `<variation_name>_alt_mem_ddrx_controller_top.v` file in an editor and change the line:

```
.CFG_ENABLE_INTR(CFG_ENABLE_INTR),  
to  
.CFG_ENABLE_INTR(CTL_ECC_ENABLED),
```


Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY.

ECC Registers Not Accessible from Controller Register Map

When you turn on the **Enable Error Detection and Correction Logic** option, the ECC control register, ECC status register, and ECC error address register are not accessible from the controller register map.

Affected configurations

This issue affects all configurations using the 11.0 version of the high-performance controller II with the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

You are unable to access the ECC control register, ECC status register, or ECC error register in the controller register map.

Workaround

There are two workaround options for this issue.

Option 1:

Enable the **Configuration and Status Register Interface** when you enable the **Error Detection and Correction Logic** option.

Option 2 (applicable to Verilog designs only):

Open the alt_mem_ddrx_controller_st_top.v file in an editor and change the line:

```
if (CTL_CSR_ENABLED == 1) begin
...
    .MEM_IF_DQS_WIDTH      (
CFG_MEM_IF_DQS_WIDTH      )
) register_control_inst (

to

if (CTL_CSR_ENABLED == 1) || CTL_ECC_CSR_ENABLED == 1) begin
...
    .MEM_IF_DQS_WIDTH      (
CFG_MEM_IF_DQS_WIDTH      ),
    .CTL_CSR_ENABLED       (
CTL_CSR_ENABLED           ),
    .CTL_ECC_CSR_ENABLED   (
CTL_ECC_CSR_ENABLED       )
) register_control_inst (
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY.

Error Related to Incorrect Syntax of Type Conversion

When you attempt to simulate a VHDL simulation model with NativeLink, compilation fails and reports an error message relating to incorrect syntax of type conversion.

Affected configurations

This issue affects all VHDL designs targeting DDR, DDR2, or DDR3 with the high-performance controller II (HPC II) and ALTMEMPHY.

Design Impact

Compilation fails.

Workaround

Use Verilog rather than VHDL.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY.

VCS Simulation Fails and Reports that Module was Previously Declared

If you set VCS as your simulator and attempt to simulate your high-performance controller II (HPC II)-based design with NativeLink, the VCS simulation fails and reports that the module was previously declared.

Affected configurations

This issue affects all high-performance controller II (HPC II)-based IP designs with ALTMEMPHY.

Design Impact

Compilation fails in VCS.

Workaround

The workaround for this issue is to perform the following steps, before running the simulation:

1. Open the `<variation_name>.v` file in an editor.
2. In the `<variation_name>.v` file, find the following text:
`// IPFS_FILES: <files list>;`
3. Remove the entire file list by replacing the text located in step 2 with the following text: `// IPFS_FILES: ;`

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY.

Half Rate Bridge Not Supported

If you open an IP design created in version 10.1 of the Quartus II software in version 11.0 and enable the Half Rate Bridge feature, the design may fail in simulation.

Affected configurations

This issue affects all 10.1 designs opened in the Quartus II software version 11.0.

Design Impact

Simulation fails.

Workaround

Do not enable the Half Rate Bridge feature.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

System Timestamp Mismatch Warning Message

A warning message similar to the following might be displayed during IP generation with SOPC Builder: system timestamp mismatch - connected: 1301987588.

Affected configurations

All ALTMEMPHY-based systems generated with SOPC Builder.

Design Impact

This issue has no design impact.

Workaround

You may ignore the displayed message.

Solution Status

This issue will not be fixed.

VHDL Example Driver Fails in Simulation

The VHDL example driver for designs using the high-performance controller (HPC) fails to simulate.

Affected configurations

This issue affects all ALTMEMPHY-based designs using the high-performance controller, and targeting VHDL.

Design Impact

The VHDL example driver fails to compile in VCS/VCSMX and hence cannot simulate.

Workaround

The workaround for this issue is to use the Verilog example driver.

Solution Status

This issue will not be fixed.

DDR3 ODT Fails in Simulation with Denali

DDR3 ODT failures can occur in simulation with Denali.

Affected configurations

This issue affects DDR3 configurations with unbuffered DIMM, multiple DIMMs, ODT enabled, and a number of slots greater than 1.

Design Impact

This issue can result in a simulation error, and can also result in data corruption in hardware.

Workaround

There are two possible workarounds for this issue:

Option 1: Open the `alt_mem_ddrx_controller_st_top.v` file and add 1 (clk) to the equation used to derive the localparams `CFG_EXTRA_CTL_CLK_RD_TO_WR_DIFF_CHIP` and `CFG_EXTRA_CTL_CLK_WR_TO_RD_DIFF_CHIP`.

Option 2: Open the generated file `<variation_name>_alt_mem_ddrx_controller_top.v` and change the localparam `CFG_READ_ODT_CHIP` value to `'h0`.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP

Resynchronization Registers Incorrectly Placed in Core instead of I/O

For designs targeting Arria II GX devices, the Quartus II software incorrectly places resynchronization registers in the core instead of the I/O.

Affected configurations

This issue affects designs targeting Arria II GX devices and using the DDR3 SDRAM Controller with ALTMEMPHY IP.

Design Impact

Possible intermittent data corruption of the last word in a burst.

Workaround

For Quartus II software versions 10.1 and 10.0SP1, download and install the Quartus II software patch described in the solution available here:
http://www.altera.com/support/kdb/solutions/rd12132010_638.html.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Devices Faster than 533MHz Require Manual Derating

The DDR3 SDRAM Controller with ALTMEMPHY provides automatic derating based on the AC175 threshold. Memory devices faster than 533 MHz require derating based on the AC150 threshold.

Affected configurations

This issue affects all configurations using memory devices faster than 533 MHz.

Design Impact

This issue can result in inaccurate timing analysis.

Workaround

You should calculate derated setup and hold values for your memory device, and enter those values in the DDR3 SDRAM Controller with ALTMEMPHY parameter editor.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY.

pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems

For systems generated with Qsys, the `<variation_name>_pin_assignments.tcl` script does not assign correct pin names. This situation occurs because the entity name assigned by Qsys is not yet known at generation time when the `<variation_name>_pin_assignments.tcl` script is generated.

Affected configurations

This issue affects all configurations.

Design Impact

Your design fails to simulate and does not work in hardware.

Workaround

After generating your IP core, edit the `<variation_name>_pin_assignments.tcl` script and change the `set instance_name` line to specify the correct name of your controller instance.

Solution Status

This issue will not be fixed.

Warning Messages Reporting Ignored SDC Constraints

During compilation of a Qsys-generated IP core, the TimeQuest Timing Analyzer may display warning messages indicating that SDC constraints are being ignored. These messages appear because TimeQuest reads the `altera_avalon_half_rate_bridge_constraints.sdc` file even though the Half Rate Bridge feature is not used.

Affected configurations

This issue affects all Qsys-generated configurations.

Design Impact

This issue has no design impact.

Workaround

To prevent display of the warning messages, remove the `altera_avalon_half_rate_bridge_constraints.sdc` file from the project and from any `.qip` file.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Error in Board Settings GUI

For Stratix III designs, the board parameters are editable in the ALTMEMPHY MegaWizard interface, but cannot be used for timing analysis.

Affected Configurations

This issue affects all designs that target the Stratix III devices.

Design Impact

Your design may be parameterized wrongly.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Using Merging Feature

When you generate designs with DDR3 high-performance controller II (HPC II), the merging feature is turned off by default. If your traffic exercises pattern that you can merge, you should turn on merging. Turning merging on may affect f_{MAX} performance.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture in version 10.0 of the DDR3 Controller with ALTMEMPHY IP.

Design Impact

If you can merge traffic when you turn on the merging feature, there is a performance improvement.

Workaround

To turn on the command merging feature, follow these steps:

1. Open the `<variation_name>_alt_ddrx_controller_wrapper.v` file.
2. Search for the `ENABLE_BURST_MERGE` parameter.
3. Change the value from 0 to 1.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Memory Controller Returns Wrong Data

For designs that use the DDR3 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder, the memory controller returns incorrect data. When you initialize the memory content with the initialization data file, the fetched memory content does not match the initialization data file. This issue does not affect operation in hardware.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder.

Design Impact

Your design fails to simulate.

Workaround

Select **CHIP-BANK-ROW-COL** for the **Local-to-Memory Address Mapping** option instead.

Solution Status

This issue will not be fixed.

Refresh to Precharge Command Timing Violation

Designs that use the DDR3 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.
2. Locate the following command:

```
cs_can_precharge_all [w_cs] = chip_idle;
```

and change to:

```
cs_can_precharge_all [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Power-Down Entry Command Timing Violation

Designs that use the DDR3 HPC II architecture with the **Enable Auto Power Down** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture with the **Enable Auto Power Down** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.

2. Locate the following command:

```
always @ (*)
begin
    cs_can_power_down [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
end

and change to:
always @ (posedge ctl_clk or negedge ctl_reset_n)
begin
    if (!ctl_reset_n)
        cs_can_power_down [w_cs] <= 1'b0;
    else
        cs_can_power_down [w_cs] <= power_saving_enter_ready [w_cs] & chip_idle;
    end
end
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Failure to Regenerate 9.0 Designs in Silent Mode

If you regenerate your version 9.0 designs in silent mode, the controller is defaulted to the HPC II architecture and triggers a “memory burst length” error.

Affected Configurations

This issue affects all version 9.0 configurations.

Design Impact

Your design fails to generate successfully.

Workaround

Open your design in version 10.0 of the DDR3 SDRAM Controller with ALTMEMPHY IP, and regenerate your design.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

CSR Address 0x005 and 0x006 Contents Cannot be Accessed

Leveled DDR3 designs that use the ALTMEMPHY-based HPC II architecture with the **Enable Configuration and Status Register Interface** option turned on, cannot access the CSR address 0x005 and 0x006 contents.

Affected Configurations

This issue affects all non-leveled designs that use the ALTMEMPHY-based HPC II architecture with the **Enable Configuration and Status Register Interface** option turned on.



The leveled DDR3 designs, such as DIMMs, also do not have access to the CSR address 0x005 and 0x006 contents, but this is because the IP is not designed to support this feature.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To access the CSR address 0x005 and 0x006 contents (discrete device only), follow these steps:

1. Open *<variation name>_controller_phy.v* file.
2. Search for the following debug ports under the *<variation name>_phy* instantiation.
 - dbg_clk (Clock)
 - dbg_addr (Address)
 - dbg_cs (Chip select)
 - dbg_waitrequest (Wait request)
 - dbg_wr (Write request)
 - dbg_wr_data (Write data)
 - dbg_rd (Read request)
 - dbg_dr_data (Read data)
3. Export these ports into *<variation name>_example.v* file.
4. Use the Avalon-MM protocol to access the CSR address 0x005 and 0x006 contents through the debug ports.

Solution Status

This issue will not be fixed.

Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate

Memory timing violation occurs during the activate to read precharge.

Affected Configurations

This issue affects all designs that use the high-performance controller architecture.

Design Impact

Your design may fail to simulate.

Workaround

For designs targeting 1066 specification and running with 533 MHz speed, increase one control clock cycle of the timing parameters **tRP** and **tRCD**, so that the tRC for the controller is greater than the tRC for the memory model.

For designs targeting 1066 specification and running with 400 MHz speed, increase one control clock cycle of the timing parameter **tRP**, so that the tRC for the controller is greater than the tRC for the memory model.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Half-Rate Clock Not Connected When Clock Sharing is Enabled

If you generate a DDR3 controller with the **High Performance Controller II** and **Multiple Controller Clock Sharing** options enabled in SOPC Builder, the half-rate clock is not connected.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Multiple Controller Clock Sharing** option enabled in SOPC Builder.

Design Impact

The internal half-rate bridge for the sharing PLL controller does not function.

Workaround

To connect the half-rate clock, perform the following steps:

1. Edit the sharing PLL controller top-level file to include the half-rate clock input port as in the following example:

■ Verilog HDL

```
module <variation name> (  
  
    sys_clk_in,  
  
    sys_half_clk_in,
```

```

soft_reset_n,
input sys_clk_in;
input    sys_half_clk_in;
input soft_reset_n;

.sys_clk_in(sys_clk_in),
.sys_half_clk_in(sys_half_clk_in),
.soft_reset_n(soft_reset_n),

```

■ VHDL

```

ENTITY <variation name_master> IS
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in    : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;

COMPONENT <variation name>_controller_phy
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in    : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;
sys_clk_in  => sys_clk_in,
sys_half_clk_in => sys_half_clk_in,
aux_full_rate_clk => aux_full_rate_clk,

```

2. Edit the SOPC top-level file to connect the half-rate clock from the source to the sharing controller as in the following example:

■ Verilog HDL

```

<variation name> the_<variation name>
(

.soft_reset_n (clk_0_reset_n),
.sys_half_clk_in    ( <variation
name_master>_aux_half_rate_clk_out),
.sys_clk_in  (<variation name_master>_phy_clk_out)

```

■ VHDL

```

component <variation name> is
port (
-- inputs:

```

```
signal soft_reset_n : IN STD_LOGIC;  
  
signal sys_half_clk_in : IN STD_LOGIC;  
  
signal sys_clk_in : IN STD_LOGIC;  
  
the_<variation name> : <variation name>  
  
port map(  
  
    soft_reset_n => clk_0_reset_n,  
    sys_half_clk_in => out_clk_<variation name_master>_aux_half_rate_clk,  
    sys_clk_in => internal_<variation name_master>_phy_clk_out
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Generate Simulation Model Option Gets Disabled

The **Generate simulation model** option gets disabled after every generation.

Affected Configurations

This issue affects all configurations.

Design Impact

The simulation model for your design is not generated for the second time.

Workaround

Turn on the **Generate simulation model** option each time you want to generate a simulation model.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Designs with Eight Chip Selects Fail Compilation

Designs that use eight chip selects with the high-performance controller architecture fail to compile.

Affected Configurations

This issue affects all designs that use eight chip selects with the high-performance controller architecture

Design Impact

Your design fails to compile.

Workaround

In the MegaWizard interface, select **High Performance Controller II** as your controller architecture.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Address Mirroring Not Supported By Memory Simulation Model

The default memory simulation model does not support address mirroring. When you generate your design in the example testbench with the address mirroring parameter enabled, your simulation fails. To simulate successfully, you must replace the current memory simulation model with a vendor memory model and mirror the address bits in the *<variation name>_example_top_tb.v* or *.vhd* file.

Affected Configurations

This issue affects the multiple chip selects DDR3 DIMM which require mirrored address bits.

Design Impact

The default memory simulation model does not support DDR3 DIMM multiple chip selects mirrored address bits. Your design fails to simulate.

Workaround

Use the vendor memory model and mirror the address bits in the example top for target chip selects by doing the following:

1. Regenerate the DDR3 testbench. After generating, in the top variant file, *<variation name>.v* or *.vhd*, look for the following code:

```
//Retrieval info: <PRIVATE name = "use_generated_memory_model" value="true"
type="STRING" enable="1"/>
```

and change to:

```
//Retrieval info: <PRIVATE name = "use_generated_memory_model"
value="false" type="STRING" enable="1"/>
```

2. Download the vendor memory model.
3. For the chip selects that require address mirroring, edit the *<variation name>_example_top_tb.v* or *.vhd* file by performing the following:

- a. Add the following lines:

```
wire[gMEM_ADDR_BITS - 1:0] a_reversed;
wire[gMEM_BANK_BITS - 1:0] ba_reversed;
assign a_reversed[2:0] = a_delayed[2:0];
assign a_reversed[3] = a_delayed[4];
assign a_reversed[4] = a_delayed[3];
assign a_reversed[5] = a_delayed[6];
```

```

assign a_reversed[6] = a_delayed[5];
assign a_reversed[7] = a_delayed[8];
assign a_reversed[8] = a_delayed[7];
assign a_reversed[gMEM_ADDR_BITS - 1:9] = a_delayed[gMEM_ADDR_BITS -
1:9];
assign ba_reversed[0] = ba_delayed[1];
assign ba_reversed[1] = ba_delayed[0];
assign ba_reversed[gMEM_BANK_BITS - 1:2] = ba_delayed[gMEM_BANK_BITS
- 1:2];

```

b. Locate the following lines:

```

.ba (ba_delayed),
.addr (a_delayed[14-1: 0]),
and change to:
.ba (ba_reversed),
.addr (a_reversed),

```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Memory Preset Parameters Do Not Get Updated

Some memory presets are changed in version 9.0 of the DDR3 SDRAM High-Performance Controller. If you migrate your existing design from version 8.1 to 9.0, your memory preset parameters do not get updated in version 9.0.

Affected Configurations

This issue affects all designs that are migrated to version 9.0.

Design Impact

The memory preset parameters in your design do not get updated in version 9.0, even if you regenerate the MegaCore function.

Workaround

In the MegaWizard GUI, choose any random memory presets, and then reselect your original presets (remember to redo any modifications to the preset such as DQ width, CAS latency, and so on). Click **Finish** to regenerate the MegaCore function.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR3 SDRAM high-performance controllers do not work with the **Enable Error Detection and Correction Logic** option enabled.

Affected Configurations

This issue affects all designs that use DDR3 SDRAM high-performance controllers that have the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

Your design does not work properly in both simulation and hardware after the subsequent reset.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Revision History

Table 12–1 shows the revision history for the FFT MegaCore function.



For more information about the new features, refer to the *FFT MegaCore Function User Guide*.

Table 12–1. FFT MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Stratix IV GT devices. Efficiency enhancements.
10.0	July 2010	<ul style="list-style-type: none"> Preliminary support for Stratix V devices. New Transform Length values.

Errata

Table 12–2 shows the issues that affect the FFT MegaCore function v11.0, v10.1 SP1, v10.1, and v10.0.



Not all issues affect all versions of the FFT MegaCore function.

Table 12–2. FFT MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		11.0	10.1 SP1	10.1	10.0
1 Jul 11	User Guide Table Lists Wrong Bit Growth for Variable Streaming Fixed Point Architecture	✓	—	—	—
15 May 11	Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices	✓	—	—	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	✓	—
15 Feb 11	Variable Streaming Floating Point Variations Cannot Simulate Inverse FFT Computation	—	Fixed	✓	—

Table 12-2. FFT MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		11.0	10.1 SP1	10.1	10.0
15 Dec 10	Variable Streaming Floating Point Variations Might Produce ± 1 Errors in Simulation	✓	✓	✓	—
	Simulation Errors—MATLAB Model Mismatch	—	—	Fixed	✓
	Some Variations with VHDL Output Files Generate Incorrect Simulation Models for Stratix V Devices	—	—	Fixed	✓
01 Dec 06	Simulation Errors—Incorrect Results	✓	✓	✓	✓

User Guide Table Lists Wrong Bit Growth for Variable Streaming Fixed Point Architecture

For variable streaming fixed point architecture, the bit growth is $\log_2(\max(\text{fftpts})) + 1$. This bit growth is listed correctly in “Variable Streaming Architecture”, on page 3-3 of the *FFT MegaCore Function v11.0 User Guide*. However, the note to Table 3-4 incorrectly lists the bit growth that is correct in versions that precede the Quartus II software v11.0.

Affected Configurations

All FFT MegaCore function variable streaming fixed point variations.

Design Impact

This issue has no design impact.

Workaround

Use the bit growth formula on page 3-3 of the user guide instead of the formula in the note to Table 3-4.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore Function User Guide.

Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices

The FFT MegaCore function v11.0 provides final support for Arria II GZ and Cyclone IV GX devices. However, when your FFT MegaCore function targets an Arria II GZ device or a Cyclone IV GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All FFT MegaCore function variations that target an Arria II GZ device or a Cyclone IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Compilation Targeting a Stratix V Device Fails

Designs that include an FFT IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

FFT IP core designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Variable Streaming Floating Point Variations Cannot Simulate Inverse FFT Computation

FFT MegaCore function variations with variable streaming floating point architecture produce errors in simulation when the inverse input signal is set to value 1. Variations with this architecture cannot simulate the inverse FFT operation correctly.

Affected Configurations

All FFT MegaCore function variations with variable streaming floating point architecture.

Design Impact

This issue has no design impact. It affects simulation only.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 Service Pack 1 of the FFT MegaCore function.

Variable Streaming Floating Point Variations Might Produce ± 1 Errors in Simulation

FFT MegaCore function variations with variable streaming floating point architecture might produce ± 1 errors in simulation output values.

Affected Configurations

All FFT MegaCore function variations with variable streaming floating point architecture.

Design Impact

This issue has no design impact. It affects simulation only.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—MATLAB Model Mismatch

For one particular FFT parameter combination, the HDL output does not match the MATLAB simulation results (for some frames of data).

HDL simulation results are scaled down by a factor of two compared to the MATLAB simulation results. The exponent value produced by the HDL simulation is one less than the output of the MATLAB simulations. When the exponent is taken into account, the MATLAB and the HDL version may differ by one LSB.

Affected Configurations

This issue affects the following parameter combination:

- Transform length: 64
- I/O data flow: burst architecture
- FFT engine architecture: quad output
- Number of parallel engines: 2

Design Impact

There is no design impact; the design compiles and operates correctly.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the FFT MegaCore function.

Some Variations with VHDL Output Files Generate Incorrect Simulation Models for Stratix V Devices

Some FFT MegaCore function variations that target a Stratix V device and are generated as VHDL output files, generate incorrect simulation models.

Affected Configurations

All FFT MegaCore function variations that use complex 18×25 multiplication and target a Stratix V device and for which VHDL is specified as the output file HDL. Variations that use complex 18×25 multiplication include variations with variable streaming fixed point architecture, large transform length, and twiddle precision less than 18 bits, and variations with a different FFT architecture, data precision of 18–25 bits, and twiddle precision less than 18 bits.

Design Impact

This issue has no design impact; it affects simulation only.

Workaround

Specify Verilog HDL as the output file language.

Solution Status

This issue is fixed in version 10.1 of the FFT MegaCore function.

Simulation Errors—Incorrect Results

When the input is defined as N bits wide, the permissible input range is from $-2^{N-1} + 1$ to $2^{N-1} - 1$. If the input contains the value -2^{N-1} , the HDL output is incorrect, and does not match the MATLAB simulation result.

Affected Configurations

This issue affects all configurations.

Design Impact

The design compiles but gives incorrect results.

Workaround

If you expect your input signal to contain the value -2^{N-1} , you should add a block in front of the FFT, which maps the value -2^{N-1} to $-2^{N-1} + 1$.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Revision History

Table 13–1 shows the revision history for the FIR Compiler.

 For information about the new features, refer to the *FIR Compiler User Guide*.

Table 13–1. FIR Compiler Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices. Updated HardCopy initialization information in Appendix A, FIR Compiler Supported Device Structures.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Stratix IV GT devices.
10.0 SP1	September 2010	Maintenance release.
10.0	July 2010	Preliminary support for Stratix V devices.

Errata

Table 13–2 shows the issues that affect the FIR Compiler v11.0, v10.1 SP1, v10.1, v10.0 SP1, and v10.0.


 Not all issues affect all versions of the FIR Compiler.

Table 13–2. FIR Compiler Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version				
		11.0	10.1 SP1	10.1	10.0 SP1	10.0
15 May 11	Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices	✓	—	—	—	—
	64-Bit Quartus II Software Cannot Simulate or Compile FIR Compiler	✓	—	—	—	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	✓	—	—
	User Guide Does not Document that Compilation Targeting a HardCopy Device Requires Removal of .hex Files	Fixed	✓	✓	✓	✓
15 Dec 10	Half-Band Decimation Filters That Use MLABs for Coefficient Storage in Stratix V Devices Fail	—	—	—	Fixed	✓
	Symmetric Interpolation Filters That Use M20K Blocks for Data Storage in Stratix V Devices Fail	—	—	—	Fixed	✓

Table 13–2. FIR Compiler Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version				
		11.0	10.1 SP1	10.1	10.0 SP1	10.0
15 July 10	FIR Filters With Large Numbers of Coefficients and Non-Symmetric Structure Do Not Generate Netlist and IPFS Model Correctly	✓	✓	✓	✓	✓
15 May 10	FIR Compiler Functional Simulation Model Is Not Generated	✓	✓	✓	✓	✓
15 Mar 09	Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional	✓	✓	✓	✓	✓
01 Oct 08	Block Memory Incorrectly Used When Logic Storage Selected	✓	✓	✓	✓	✓
01 Oct 07	Simulation Result Incorrect Using MCV Interpolation Filters	✓	✓	✓	✓	✓
01 May 07	Reloadable Coefficient Filters Fail for Some MCV Filters	✓	✓	✓	✓	✓
01 Dec 06	Quartus II Simulation Vector File Not Generated	✓	✓	✓	✓	✓

Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices

The FIR Compiler v11.0 provides final support for Arria II GZ and Cyclone IV GX devices. However, when your FIR Compiler targets an Arria II GZ device or a Cyclone IV GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All FIR Compiler variations that target an Arria II GZ device or a Cyclone IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

64-Bit Quartus II Software Cannot Simulate or Compile FIR Compiler

The 64-bit Quartus II software installation cannot generate a functional simulation model for any variation of the FIR Compiler and cannot compile the FIR Compiler, because it does not generate the expected netlist.

When the software attempts to generate a FIR Compiler functional simulation model, the following error message displays:

```
IP Functional Simulation Model Creation Failed. The following error was
returned: Error: Node instance "fircore" instantiates undefined entity
"<instance_name>_st" File
```


When the software attempts to compile a design that includes a FIR Compiler instance, the following error message displays:

```
Error: Node instance "fircore" instantiates undefined entity  
"<instance_name>_st"
```

Affected Configurations

This issue affects all FIR Compiler variations.

Design Impact

The FIR Compiler netlist is not generated.

Workaround

To avoid this issue, install and use the 32-bit Quartus II software.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Compilation Targeting a Stratix V Device Fails

Designs that include a FIR Compiler and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

FIR Compiler designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

User Guide Does not Document that Compilation Targeting a HardCopy Device Requires Removal of .hex Files

In the *FIR Compiler User Guide*, Appendix A, FIR Compiler Supported Device Structures, the section “HardCopy II Support” should refer to all supported HardCopy devices instead of HardCopy II devices only. In particular, the instructions to remove the memory initialization .hex files from the Quartus II project directory before compiling apply to all device families in the HardCopy series of devices.

Affected Configurations

All designs that target a HardCopy device family and use memory initialization files.

Design Impact

If you apply the instructions in the Appendix only to HardCopy II devices, as stated, your HardCopy design does not compile successfully.

Workaround

To ensure your FIR compiler design that targets a HardCopy device family can compile successfully, remove the relevant .hex file from the Quartus II project directory before compiling.

Solution Status

This issue is fixed in version 11.0 of the *FIR Compiler User Guide*.

Half-Band Decimation Filters That Use MLABs for Coefficient Storage in Stratix V Devices Fail

Half-band decimation filters that target a Stratix V device and use MLABs for code storage cannot generate a netlist successfully.

Affected Configurations

Half-band decimation filters with multicycle variable structure and **Coefficient Storage** set to **MLAB** that target a Stratix V device.

Design Impact

The Quartus II software cannot generate a netlist.

Workaround

For half-band decimation filters with multicycle variable structure that target a Stratix V device, set **Coefficient Storage** to **Auto**.

Solution Status

This issue is fixed in version 10.0 SP1 of the FIR Compiler.

Symmetric Interpolation Filters That Use M20K Blocks for Data Storage in Stratix V Devices Fail

Symmetric interpolation filters that target a Stratix V device and use M20K memory blocks for data storage fail in simulation or compilation.

Affected Configurations

Symmetric interpolation filters with multicycle variable structure and **Data Storage** set to **M20K** that target a Stratix V device.

Design Impact

The Quartus II software cannot generate a netlist, or simulation fails due to a mismatch with expected results.

Workaround

For symmetric interpolation filters with multicycle variable structure that target a Stratix V device, set **Data Storage** to **Auto**.

Solution Status

This issue is fixed in version 10.0 SP1 of the FIR Compiler.

FIR Filters With Large Numbers of Coefficients and Non-Symmetric Structure Do Not Generate Netlist and IPFS Model Correctly

FIR filters with large numbers of coefficients and with **Force Non-Symmetric Structure** turned on, cannot generate a netlist successfully.

Affected Configurations

FIR filters with large numbers of coefficients and with **Force Non-Symmetric Structure** turned on.

Design Impact

The Quartus II software cannot generate a netlist or an IP functional simulation model.

Workaround

For FIR filters with **Force Non-Symmetric Structure** turned on, restrict the set of coefficients to 1500 or fewer.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

FIR Compiler Functional Simulation Model Is Not Generated

When you try to generate a FIR Compiler functional simulation model, one of the following two error messages appears:

```
"Cannot run program
"<Quartus II IP installation>\fir_compiler\lib\ip_toolbench\netlist_writer.exe"
(in directory <project directory> create process error=14001 this
application has failed to start because the application configuration is
incorrect"
```

or

```
"IP Functional Simulation Model Creation Failed. The following error was
returned: Error: Node instance "fircore" instantiates undefined entity
"<instance_name>_st" File ..."
```

and the functional simulation model is not generated.

Affected Configurations

All FIR Compiler variations.

Design Impact

FIR Compiler simulation model is not generated.

Workaround

To avoid this problem, perform the following steps:

1. Download the appropriate version of Microsoft Visual C++ 2008 SP1 Redistributable Package — (x86) for a 32-bit machine or (x64) for 64-bit Windows XP.
2. Double-click on the **vcredisk_x86.exe** or **vcredisk_x64.exe** file you downloaded.
3. Follow the instructions.



If you are prompted to uninstall or repair, click **Repair**.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional

Incorrect results when **Structure** is set to **Distributed Arithmetic: Multi-Bit Serial Filter** or the **Rate Specification** is set to **Interpolation**, and **Signed Binary Fractional** is specified for the data type.

Affected Configurations

Configurations that have a signed binary fractional data type with either a multi-bit structure or an interpolation filter rate specification.

Design Impact

The output data is incorrect.

Workaround

Avoid using a multi-bit serial structure or an interpolation filter rate specification with signed binary fractional data types.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Block Memory Incorrectly Used When Logic Storage Selected

For some instances of the FIR Compiler MegaCore function, if you select logic-based storage for data and coefficients, it is possible that the results of synthesis may include some block memory.

Affected Configurations

Configurations with FIR storage set to logic elements.

Design Impact

An unwanted block memory is used.

Workaround

Turn off **Auto Shift Register Replacement** in the Quartus II **More Analysis and Synthesis Settings** dialog box. This dialog box can be accessed by clicking **More Settings** in the **Analysis & Synthesis Settings** page of the **Settings** dialog box accessed from the Assignments menu in the Quartus II software.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Simulation Result Incorrect Using MCV Interpolation Filters

Some multicycle variable interpolation filters with high interpolation factors may generate incorrect output.

Affected Configurations

This issue affects MCV interpolation filters with high interpolation factors and forced non-symmetric implementation where the pipelining level is set to greater than 1 for higher f_{MAX} .

Design Impact

The produced output does not match the expected output.

Workaround

Change the pipelining level to 1. This change may result in lower f_{MAX} but the filter output will match the expected output.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Reloadable Coefficient Filters Fail for Some MCV Filters

Some reloadable coefficient filters with multicycle variable architecture do not produce the right output when a new set of coefficients is reloaded.

Affected Configurations

This error is observed in some of the reloadable coefficient MCV filters.

Design Impact

The produced output does not match the expected output when the new coefficient set is reloaded.

Workaround

There are two separate problems which may cause this failure. If your target device is **Cyclone III**, change the device to **Stratix II** or **Stratix III** in the FIR Compiler GUI and regenerate the filter. (Your device selection in the Quartus II project should stay the same). If the coefficient storage is set to logic cells, change to a block memory (such as **M512**, **M9K**, or **Auto**).

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Quartus II Simulation Vector File Not Generated

FIR Compiler does not create a vector file for Quartus II simulation.

Affected Configurations

This issue affects all configurations.

Design Impact

The design can be compiled, but there is no automatically generated vector file testbench available to simulate the design in the Quartus II software.

Workaround

Use NativeLink to simulate the VHDL testbench instead.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Revision History

Table 14–1 shows the revision history for the FIR Compiler II.


 For information about the new features, refer to the *FIR Compiler II User Guide*.

Table 14–1. FIR Compiler II Revision History

Version	Date	Description
11.0	May 2011	Added resource utilization and performance information for Stratix V devices.
10.1	December 2010	Added new output options and multiple coefficient banks feature.
10.0	July 2010	Added backpressure and coefficient reloading features.

Errata

Table 14–2 shows the issues that affect the FIR Compiler II v11.0, v10.1, and v10.0.


 Not all issues affect all versions of the FIR Compiler II.

Table 14–2. FIR Compiler II Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	Parameter Editor Stops Responding	✓	—	—
15 Dec 10	Unable to Run FIR Compiler II	✓	✓	✓
15 Jul 10	NativeLink is Not Supported	Fixed	Fixed	✓
15 Feb 10	Simulation Fails with Single-Language Simulator	✓	✓	✓
	M144K Memories Output X's in the ModelSim-Altera Software	✓	✓	✓
	Incorrect Testbench Result When Interpolation Factor Is Greater Than The TDM Factor	—	—	Fixed
	Incorrect Results for a Decimation Configuration	—	—	Fixed
	Incorrect Results Might Be Produced When Input Bit Width is Greater Than 17 bits.	—	—	Fixed
	Simulation fails with the NCSim/Riviera-Pro/ActiveHDL Simulator	—	—	Fixed
	Compiler Does Not Create a Block Symbol File	Fixed	Fixed	✓

Parameter Editor Stops Responding

The FIR Compiler II parameter editor stops responding when you specify a high Input Sample Rate or a high Input Sample Rate/Clock Rate ratio.

Affected Configurations

This issue affects the FIR Compiler II parameter editor when you specify Input Sample Rate > 10000 or Input Sample Rate/Clock Rate > 500.

Design Impact

The FIR Compiler II MegaCore function cannot be generated.

Workaround

To avoid this problem, use Input Sample Rate < 10000 or Input Sample Rate/Clock Rate < 500.

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Unable to Run FIR Compiler II

The FIR Compiler II MegaCore fails to run with the following error message:

```
Error: couldn't execute"<Quartus installation  
path>\quartus\common\ip\altera\windows32\fir_ip_api_interface": no such  
file or directory.
```

Affected Configurations

This issue affects all FIR Compiler II variations.

Design Impact

The FIR Compiler II Core cannot be generated.

Workaround

To avoid this problem, follow these steps:

1. Download the appropriate version of Microsoft Visual C++ 2008 SP1 Redistributable Package — (x86) for a 32-bit machine or (x64) for 64-bit Windows XP.
2. Double-click on the `vcredisk_x86.exe` or `vcredisk_x64.exe` file you downloaded.
3. Follow the instructions.



If you are prompted to uninstall or repair, click **Repair**.

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

NativeLink is Not Supported

Unable to perform simulation using NativeLink.

Affected Configurations

This issue affects all simulators supported by NativeLink.

Design Impact

The design does not simulate.

Workaround

Use Modelsim SE or Modelsim AE to run simulation.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.1.

Simulation Fails with Single-Language Simulator

When the ModelSim® AE or any single-language simulator is used, the simulation fails because FIR Compiler II is written in both Verilog and VHDL.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Use the quartus_map API at the command line to create a simulation model by typing the following command:

```
quartus_map <variant file name> --simgen --  
simgen_parameter="CBX_HDL_LANGUAGE=<language>"  
language : VHDL / VERILOG
```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

M144K Memories Output X's in the ModelSim-Altera Software

The simulation fails if the M-RAM memory threshold is set inappropriately.

Affected Configurations

This issue affects all configurations if the M-RAM threshold is set to a small value.

Design Impact

The simulation fails due to the output X's produced by the M144K memories.

Workaround

Set the M-RAM threshold to the default value (for example, set the value to 1000000)

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Incorrect Testbench Result When Interpolation Factor Is Greater Than The TDM Factor

The testbench produces incorrect results when the filter is configured with interpolation factor greater than the TDM factor (the ratio of the clock rate to the sample rate).

Affected Configurations

This issue affects configurations with interpolation factor greater than the TDM factor.

Design Impact

There is no design impact. This is a testbench issue.

Workaround

Set the interpolation factor equals or lesser than the TDM factor.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Incorrect Results for a Decimation Configuration

Incorrect results are produced when the filter is configured as decimation type with certain parameters.

Affected Configurations

This issue affects the following parameter combination:

- Decimation Factor: 2
- Coefficient Bit Width: 8
- Symmetry Mode: Non Symmetry

Design Impact

The output data is incorrect.

Workaround

Use different coefficient bit width or symmetry mode when you use decimation by two configuration.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Incorrect Results Might Be Produced When Input Bit Width is Greater Than 17 bits.

Incorrect results might be produced when you set the input bit width other than 1–17 bits.

Affected Configurations

Configurations with input bit width greater than 17 bits.

Design Impact

The output data is incorrect.

Workaround

Set the input bit width within 1–17 bits.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Simulation fails with the NCSim/Riviera-Pro/ActiveHDL Simulator

When you run design simulations with NCSim/Riviera-Pro/ActiveHDL, the simulations might fail with the following error message on the respective softwares.

```
Verilog module/VHDL port width mismatch -
ALTERA_AVALON_SC_FIFO.OUT_EMPTY. (NCSIM). Length of connection (0)
does not match the length of port "out_empty" (2) on instance.
(Riviera-Pro)

Fatal Error: ELAB2_0051 auk_dspip_avalon_streaming_sink_hpfr.vhd
(525): Length of connection (0) does not match the length of port
"out_empty" (2) on instance (Active-HDL)
```

Affected Configurations

This issue affects configurations with PHYSCHANIN = 1.

Design Impact

The design does not simulate.

Workaround

Remove the following lines from `auk_dspip_avalon_streaming_sink_hpfr.vhd`:

```
signal out_empty : OUT STD_LOGIC_VECTOR
(log2_ceil(DATA_PORT_COUNT)-1 DOWNT0 0);

out_empty => open,
```

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Compiler Does Not Create a Block Symbol File

The FIR Compiler II does not automatically create a Block Symbol File (`.bsf`) for the MegaCore function.

Affected Configurations

This issue affects all FIR Compiler II MegaCore function variations.

Design Impact

There is no design impact.

Workaround

In the Quartus II software, open `<variation_name>.<v|vhd>`. From the File menu, select **Create/Update** and then click **Create Symbol Files for Current File** to generate the `.bsf` file. Alternatively, use the `quartus_map` API at the command line to create the symbol file, by typing the following command:

```
quartus_map --generate_symbol=<variation_name>.<v|vhd>
```

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.1.

Revision History

Table 15–1 shows the revision history for the Interlaken MegaCore function.



For information about the new features, refer to the *Interlaken MegaCore Function User Guide*.

Table 15–1. Interlaken MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	Maintenance release.
10.1	December 2010	Initial release.

Errata

Table 15–2 shows the issues that affect the Interlaken MegaCore function v11.0 and v10.1.



Not all issues affect all versions of the Interlaken MegaCore function.



For Qsys errata, which might affect the Interlaken MegaCore function and other IP cores, refer to the *Quartus II Software Release Notes*.

Table 15–2. Interlaken MegaCore Function Errata

Added or Updated	Issue	Affected Version	
		11.0	10.1
15 May 11	SDC File Includes Overly Aggressive Timing Path Cuts	Fixed	✓
	10.3125-Gbps Variation with Transceivers Runs at Incorrect Lane Rate	Fixed	✓
15 Jan 11	rxt_rxd Warning for 10- and 20-lane Variations With Transceivers	✓	✓
15 Dec 10	Compiler Warnings When Transceivers are Excluded	✓	✓
	Critical Warnings for 12- and 20-lane Variations Without Transceivers	✓	✓
	C106 Warnings for 10- and 20-lane Variations With Transceivers	✓	✓
	Aldec Riviera-PRO Simulator Cannot Simulate Interlaken 8-lane Variation	✓	✓

SDC File Includes Overly Aggressive Timing Path Cuts

The Synopsys Design Constraints Files (.sdc) provided with the Interlaken MegaCore function cut all timing relationships between clocks. This constraint is not overly aggressive for the design examples, but it does not provide a good example for developing a customer design.

Affected Configurations

This issue affects all Interlaken MegaCore function variations.

Design Impact

This issue might cause your design to not function correctly in hardware.

Workaround

In your own design, ensure you do not cut timing paths gratuitously. Do not rely on the .sdc files provided with the IP core for examples of how to make only the necessary timing path cuts.

Solution Status

This issue is fixed in version 11.0 of the Interlaken MegaCore function.

10.3125-Gbps Variation with Transceivers Runs at Incorrect Lane Rate

The 10.3125-Gbps Interlaken MegaCore function variations require a different ref_clk frequency than they were originally designed for. If you use the MegaCore function as generated, the lane rate is 10.2 Gbps rather than 10.3125 Gbps. Therefore, in addition to running the ref_clk input clock at 322.265625 MHz as specified in the *Interlaken MegaCore Function User Guide*, you must also make some manual modifications to several of the RTL files.

Affected Configurations

All 10.3125-Gbps Interlaken MegaCore function variations with transceivers.

Design Impact

The 12-lane, 10-Gbps variation runs at 10.2 Gbps instead of the documented 10.3125 Gbps, in simulation and when programmed on the device.

Workaround

After you generate your Interlaken variation and before you simulate your design, follow these steps to modify your RTL files to fix the underlying problem:

1. Edit the file `alt_ntrlkn_gxb_10g.v` with the correct values to match the 322.265625-MHz ref_clk frequency by following these steps:
 - a. To set the correct effective data rate, replace every instance of 10200 with 10312.5.
 - b. To set the correct input period, replace every instance of 3137 with 3103.
 - c. To set the correct input clock frequency, replace every instance of 318.75 with 322.265625.
2. Edit the `submodules/<variation>.sdc` file with the correct clock frequencies by following these steps:
 - a. Set the tx_mac_c_clk frequency to 257.81 MHz.
 - b. Set the rx_mac_c_clk frequency to 257.81 MHz.

3. If you are using the Qsys design example provided with the Interlaken IP installation, follow these additional steps:
 - a. In the `alt_interlaken_12lane_10g.sdc` file in the project directory, set the following clock frequencies:
 - Sample Channel Client clock frequencies to 257.81 MHz
 - `tx_mac_c_clk` frequency to 257.81 MHz
 - `rx_mac_c_clk` frequency to 257.81 MHz
 - `ref_clk` frequency to 322.265625 MHz
 - b. In the `testbench/alt_interlaken_12lane_10g_tb.sv` file, update the `ref_clk` frequency by replacing `#1568` with `#1551.5`.

Solution Status

This issue is fixed in version 11.0 of the Interlaken MegaCore function.

rxt_rxd Warning for 10- and 20-lane Variations With Transceivers

When you compile an Interlaken MegaCore function 10- or 20-lane variation with transceivers, the following warning message appears:

```
Warning: Verilog HDL or VHDL warning at alt_ntrlkn_hsio_bank_pmad5.v(92):  
object "rst_rxd" assigned a value but never read
```

Affected Configurations

All 10- and 20-lane Interlaken variations with transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Compiler Warnings When Transceivers are Excluded

When you compile an Interlaken MegaCore function variations that excludes transceivers, the following warning message appears:

```
Warning: Output pins are stuck at VCC or GND  
Warning (13410): Pin "common_rx_c_clk" is stuck at GND
```

Affected Configurations

All Interlaken MegaCore function variations that exclude transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Critical Warnings for 12- and 20-lane Variations Without Transceivers

When you compile an Interlaken MegaCore function 12- or 20-lane variation that excludes transceivers, the following warning message appears:

```
Critical Warning: (High) Rule C105: Clock signal should be a global signal.  
Found <num> node(s) related to this rule.
```

The warning message includes a list of rx_lane_clk<n>_export[</>] signals, and if the out-of-band flow control block is included, some clock signals from that block.

Affected Configurations

All Interlaken MegaCore function 12- and 20-lane variations that exclude transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

C106 Warnings for 10- and 20-lane Variations With Transceivers

When you compile an Interlaken MegaCore function 10- or 20-lane variation with transceivers, the following warning message appears:

```
Warning: (Medium) Rule C106:Clock signal source should not drive registers  
triggered by different clock edges.
```

Affected Configurations

All 10- and 20-lane Interlaken variations with transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Aldec Riviera-PRO Simulator Cannot Simulate Interlaken 8-lane Variation

The Aldec, Inc. Riviera-PRO simulator cannot simulate an Interlaken MegaCore function eight-lane variation correctly.

Affected Configurations

All eight-lane Interlaken MegaCore function variations.

Design Impact

This issue has no design impact. The problem affects simulation only.

Workaround

Use a different simulator to simulate your design, if it includes an eight-lane Interlaken MegaCore function variation.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Revision History

Table 16–1 shows the revision history for the Interlaken PHY IP core.


 For more information about the new features, refer to the “Interlaken PHY IP Core” chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 16–1. Interlaken PHY Revision History

Version	Date	Description
11.0	May 2011	Quartus II 11.0 software release.
10.1	December 2010	Added simulation support in ModelSim SE, Synopsys VCS MX, Cadence NCSim Changed number of lanes supported from 4–24 to 1–24.
10.0 SP1	September 2010	Added simulation support.
10.0	July 2010	First release.

Errata

Table 16–2 shows the issues that affect the Interlaken PHY IP core in versions 11.0, 10.1, and 10.0.

Table 16–2. Interlaken PHY Errata

Added or Updated	Issue	Affected Version	
		11.0	10.1
15 Dec 10	Mixed Language Simulation Fails when Optimization Is On	✓	✓

Mixed Language Simulation Fails when Optimization Is On

Simulation fails when using ModelSim with mixed-languages.

Affected Configurations

This issue affects mixed language simulation including Verilog modules and VHDL entities when optimization is on.

Workaround

The workaround is to turn ModelSim optimization off by using the `-novpt` option to the `vsim` command.

Solution Status

This issue may be fixed in a future version of ModelSim.

Revision History

Table 17–1 shows the revision history for the IP Compiler for PCI Express.



For complete information about the new features, refer to the *IP Compiler for PCI Express User Guide*.

Table 17–1. IP Compiler for PCI Express Revision History

Version	Date	Description
11.0 SP1	July 2011	<ul style="list-style-type: none"> Maintenance release.
11.0	May 2011	<ul style="list-style-type: none"> Name change to <i>IP Compiler for PCI Express</i>. Removed support for Stratix V devices. Stratix V device support is provided by the <i>Stratix V Hard IP for PCI Express</i>, and not by the <i>IP Compiler for PCI Express</i>. Added Qsys support.
10.1 SP1	February 2011	<ul style="list-style-type: none"> Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> Added following new features to Stratix V support: <ul style="list-style-type: none"> 256-bit interface. Target design example demonstrating the 256-bit interface that connects the PCI Express IP core to a root complex and a downstream application with the 256-bit interface. Verilog HDL and VHDL simulation support. Added support for the Gen1 ×1 soft IP implementation in Cyclone IV GX device with the Avalon-ST interface. Added support for the hard IP implementation in the Arria II GZ device with the Avalon-ST interface and the following capabilities: <ul style="list-style-type: none"> Gen1 ×1, ×4 64-bit interface, Gen1 ×8 128-bit interface. Gen2 ×1, 64-bit interface, Gen2 ×4, 128-bit interface.
10.0 SP1	September 2010	<ul style="list-style-type: none"> Added support for the soft IP implementation of the PCI Express MegaCore function in Cyclone IV E devices. Added simulation support for the hard IP implementation of the PCI Express MegaCore function in Stratix V devices. Added support for the Gen2 ×8 design example described in the “Testbench and Design Example” chapter of the <i>PCI Express Compiler User Guide</i>.
10.0	July 2010	<ul style="list-style-type: none"> Preliminary support for ×1, ×4, ×8 Gen1 and Gen2 PCI Express MegaCore function in Stratix V devices Added new, integrated PCI Express hard IP endpoint variant that includes all reset and calibration logic Added new, light-weight PCI Express completer-only endpoint variant with fixed transfer size of a single dword

Errata

Table 17-2 shows the issues that affect the IP Compiler for PCI Express in versions 11.0 SP1, 11.0, 10.1 SP1, 10.1, 10.0 SP1, and 10.0.



Not all issues affect all versions of the IP Compiler for PCI Express.

Table 17-2. IP Compiler for PCI Express Errata (Part 1 of 2)

Added or Updated	Issue	Affected Versions					
		11.0 SP1	11.0	10.1 SP1	10.1	10.0 SP1	10.0
15 Jul 11	Root Port Bus Functional Model (BFM) and Endpoint Design Example Not Available	✓	—	—	—	—	—
	User Guide Does Not Include Pin Assignments in Qsys Design Example	✓	✓	—	—	—	—
1 Jul 11	IP Core Might Exceed Maximum ACK Latency When ASPM L0s is Enabled in Stratix IV Devices	✓	✓	✓	✓	✓	✓
	IP Compiler for PCI Express Stratix IV GX Reset Controller Does Not Enter Recovery Immediately if Reference Clock Constraints are Not Met	✓	✓	—	—	—	—
15 May 11	SOPC Builder-Generated Hard IP Variations Might Violate FC Update Frequency Requirement	✓	✓	✓	✓	✓	✓
	User Guide Specifies Wrong Arria II GX Support for Avalon-MM 62.5 MHz Application Clock	—	Fixed	✓	✓	✓	✓
	ModelSim-Altera Simulation of IP Compiler for PCI Express is Slow	✓	✓	—	—	—	—
	User Guide Incorrectly Shows Support for Avalon-MM Interface in Multiple Device Families	—	Fixed	✓	✓	✓	✓
	Qsys-Generated VHDL Testbench Cannot Simulate	✓	✓	—	—	—	—
	User Guide and Parameter Editor Allow Incorrect Application Clock Frequency for Stratix V GX Devices	—	—	✓	✓	✓	✓
	Hold Time Violations for Hard IP Variations on Arria II GZ Devices	—	Fixed	✓	✓	—	—
	PCI Express IP Core Cannot Negotiate to Gen 2 Data Rate on Some Devices	✓	✓	✓	✓	✓	✓
	Incorrect Arria II GZ Device Support in User Guide	—	Fixed	✓	✓	—	—
	User Guide Incorrectly Includes an ALTGX B Reset Signal	✓	✓	✓	✓	—	—
	Incorrect Numbering of 256-Bit Interface in User Guide	—	Fixed	✓	✓	—	—
	User Guide Does Not Clarify that Posted Requests and Completions May Be Blocked if rx_st_mask Is Asserted	—	Fixed	✓	✓	✓	✓
	Incorrect Connections Shown in SOPC Builder Illustration	—	Fixed	✓	✓	✓	✓
15 Feb 11	Memory Read Requests Hang in the SOPC Builder Soft IP Implementation	—	—	Fixed	✓	✓	✓

Table 17–2. IP Compiler for PCI Express Errata (Part 2 of 2)

Added or Updated	Issue	Affected Versions					
		11.0 SP1	11.0	10.1 SP1	10.1	10.0 SP1	10.0
15 Dec 10	Root Port Example Design Simulation Fails for Some Versions of ModelSim	—	—	—	Fixed	✓	✓
	VCS Simulation Script Fails for PCIe Root Port Design Example	—	—	—	Fixed	✓	✓
	SOPC Builder Hard IP Implementation Hangs when Entering L1 State	—	—	—	Fixed	✓	✓
	The Transceiver May Be Incorrectly Reset Leading to Unreliable Link Behavior	—	—	—	Fixed	✓	✓
	Timing Analysis for Cyclone IV GX ×1 Variants	—	—	—	Fixed	✓	✓
	PCI Express Compliance Test Does Not Generate Gen2 Compliance Pattern	—	—	—	Fixed	✓	✓
15 Sept 10	Arria II GX Missing PLL_powerdown Signal when Using Custom Quartus II Installation	✓	✓	✓	✓	✓	✓
	Compilation Fails for Hard IP PCI Express MegaCore Function in Stratix IV GT Devices	—	—	—	—	Fixed	✓
	PCI Express Hard IP Compilation Is Disabled for Gen1 ×4 and ×8 in Some Devices	—	—	—	—	Fixed	✓
	PCI Express Design Example Does Always Not Close Timing in Stratix V GX and HardCopy IV GX in 250 MHz Modes	—	—	—	—	Fixed	✓
01 Apr 10	MSI Requests not Supported in Completer Only Mode	✓	✓	✓	✓	✓	✓
	Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Variation File	✓	✓	✓	✓	✓	✓

Root Port Bus Functional Model (BFM) and Endpoint Design Example Not Available

The root port BFM and endpoint design example are not available for simulation in version 11.0 SP1 of the Quartus II software. If you begin simulation, the following message displays, “BFM model not available.”

Affected Configurations

This issue affects the root port and endpoint design examples described in the “Testbench and Design Example” and “SOPC Builder Design Example”, and “Qsys Design Example” chapters of the *IP Compiler for PCI Express User Guide*.

Workaround

The workaround is use a third-party BFM for simulation.

Solution Status

For the 11.0 SP1 release, the solution is to purchase a third-party BFM.

User Guide Does Not Include Pin Assignments in Qsys Design Example

To add pin assignments to your Quartus II project, you must source the Tcl file explicitly in the Quartus II Tcl Console before compiling the project. However, the instructions to run the Qsys design example in the *IP Compiler for PCI Express User Guide* do not describe this step. If you skip this step, the Qsys design example does not compile with the required pin assignments.

In addition, the Tcl script for the Qsys design example version 11.0 contains some typos which are addressed in the Workaround section.

Affected Configurations

This issue affects the Qsys design example described in Chapter 17, "Qsys Design Example" in the *IP Compiler for PCI Express User Guide*.

Workaround

To avoid this issue, add the following step in the instructions to compile the Qsys design example Quartus II project, in the "Compiling the Design" section of Chapter 17, "Qsys Design Example" in the *IP Compiler for PCI Express User Guide*:

After you open the **s4gx_gen1x8_qsys_top.qpf** project and before you click **Start Compilation**, follow these steps 2 and 3 between the current step 1 and step 2 in the user guide:

2. In a text editor, open the file **s4gx_gen1x8_qsys_top.tcl** and make and save the following changes:
 - Comment out all lines that precede the following line:


```
set_global_assignment -name FAMILY "Stratix IV"
```
 - Replace the following line:


```
set_global_assignment -name QIP_FILE hip_s4gx_gen1x8_qsys.qip
```

 with the replacement line


```
set_global_assignment -name QIP_FILE \
  hip_s4gx_gen1x8_qsys/synthesis/hip_s4gx_gen1x8_qsys.qip
```
 - Search for **PARTITION_HIERARCHY** and insert the following line immediately preceding the **PARTITION_HIERARCHY** command:


```
set_instance_assignment -name INPUT_TERMINATION OFF -to refclk
```
 - Comment out the **project_close** command in the final line.
3. To apply Quartus II pin assignments, type the following command at the Tcl console command prompt:

```
source s4gx_gen1x8_qsys_top.tcl ←
```



To display the Quartus II Tcl Console, on the View menu, point to **Utility Windows** and click **Tcl Console**.

Solution Status

This issue will be fixed in a future version of the *IP Compiler for PCI Express User Guide*.

IP Core Might Exceed Maximum ACK Latency When ASPM L0s is Enabled in Stratix IV Devices

ACK Latency is the maximum latency from request receipt to acknowledgement transmission. When ASPM L0s is enabled, the ACK latency might exceed the PCI Express specification limit. This violation can occur when acknowledgement data link layer packets compete with TX transaction layer packets for link access during periods of high TX link utilization. If ASPM L0s is enabled and the link partner requires a high FTS count, the ACK latency can be sufficiently high to trigger retransmission of TX transaction layer packets.

Affected Configurations

This issue affects IP Compiler for PCI Express implementations with ASPM L0s enabled that target a Stratix IV device.

Workaround

To avoid this issue, disable ASPM L0s in your system.

Solution Status

This issue will be fixed in a future version of the IP Compiler for PCI Express.

IP Compiler for PCI Express Stratix IV GX Reset Controller Does Not Enter Recovery Immediately if Reference Clock Constraints are Not Met

The reset controller logic for the IP Compiler for PCI Express hard IP implementation with internal reset modules on Stratix IV GX devices does not monitor the `p1l1_locked` state after the `busy_altgxb_reconfig` signal is deasserted. As a result, you may observe link instability before the IP Compiler for PCI Express goes into link recovery following loss of PLL lock.

Affected Configurations

This issue affects all IP Compiler for PCI Express hard IP implementations with internal reset modules on Stratix IV GX devices.

Workaround

To avoid this issue, ensure your IP Compiler for PCI Express transceiver reference clock meets the following requirements:

- The reference clock must be a free running clock that is valid after the device powers up.
- The reference clock must remain stable during normal operation, soft reset, hot reset, powerdown, Link Down state, and other expected situations.

Solution Status

This issue will not be fixed in a future version of the IP Compiler for PCI Express. Correct operation requires that the design follow the reference clock constraints described in the Workaround section.

SOPC Builder-Generated Hard IP Variations Might Violate FC Update Frequency Requirement

The PCI Express specification requires that flow control information be updated every $30\ \mu\text{s} \pm 50\%$. Some SOPC Builder-generated IP Compiler for PCI Express hard IP implementations might violate that requirement for low priority FC updates. This violation can occur if a high priority FC update and a low priority FC update are scheduled to be transmitted at the same time. In this case, the low priority FC update might not be transmitted by the endpoint. However, this issue does not impact hardware performance.

Affected Configurations

This issue affects IP Compiler for PCI Express hard IP implementations generated in SOPC Builder.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the IP Compiler for PCI Express.

User Guide Specifies Wrong Arria II GX Support for Avalon-MM 62.5 MHz Application Clock

IP Compiler for PCI Express Gen1: \times 1 soft IP variations that support an Avalon-MM interface and target an Arria II GX device can support a 62.5 MHz application clock, but hard IP variations that support an Avalon-MM interface and target an Arria II GX device do not support a 62.5 MHz application clock. This support status is not documented accurately in the user guide.

Affected Configurations

All SOPC Builder- and Qsys-generated IP Compiler for PCI Express variations that target an Arria II GX device.

Workaround

No workarounds are required. This is a documentation error only.

Solution Status

This issue is fixed in version 11.0 of the *IP Compiler for PCI Express User Guide*.

ModelSim-Altera Simulation of IP Compiler for PCI Express is Slow

Simulation that uses the PCI Express BFM, or simulation of an IP Compiler for PCI Express variation that targets a Stratix IV GX or Arria II GX device, is slow in the ModelSim-Altera simulator.

Affected Configurations

This issue affects simulation of all IP Compiler for PCI Express variations when the simulator runs the PCI Express BFM, and simulations of variations that target a Stratix IV GX device that do not run the BFM.

Workaround

This issue has no workaround. You can use a different simulator to simulate your design.

Solution Status

This issue will be fixed in a future version of the IP Compiler for PCI Express.

User Guide Incorrectly Shows Support for Avalon-MM Interface in Multiple Device Families

Table 1-9 in the *PCI Express Compiler User Guide* incorrectly shows support for an Avalon-MM interface in variations that target the Cyclone II, Cyclone III, Stratix II, and Stratix III device families. However, variations that target these device families do not support an Avalon-MM interface.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue is fixed in version 11.0 of the *IP Compiler for PCI Express User Guide*.

Qsys-Generated VHDL Testbench Cannot Simulate

Qsys cannot generate a functional VHDL testbench for an IP Compiler for PCI Express.

Affected Configurations

This issue affects all IP Compiler for PCI Express variations generated in Qsys with a VHDL testbench.

Workaround

Generate and simulate your design with the Verilog HDL testbench.

Solution Status

This issue will be fixed in a future version of the IP Compiler for PCI Express.

User Guide and Parameter Editor Allow Incorrect Application Clock Frequency for Stratix V GX Devices

Gen1 x1 IP Compiler for PCI Express hard IP variations that target a Stratix V GX device support application clock frequency 125 MHz only. However, Table 4-1 in the *PCI Express Compiler User Guide* incorrectly indicates that this clock can also have frequency 62.5 MHz, and the PCI Express parameter editor allows the selection of 62.5 MHz or 125 MHz for this clock.

Affected Configurations

All Gen1 x1 PCI Express compiler hard IP variations that target a Stratix V GX device.

Workaround

For these variations, select application clock frequency 125 MHz in the PCI Express compiler parameter editor.

Solution Status

This issue is no longer relevant in version 11.0 of the IP Compiler for PCI Express and the *IP Compiler for PCI Express Compiler User Guide*. Stratix V device support is moved to the Stratix V Hard IP for PCI Express and the *Stratix V Hard IP for PCI Express User Guide*.

Hold Time Violations for Hard IP Variations on Arria II GZ Devices

IP Compiler for PCI Express hard IP variations that target an Arria II GZ device have hold time violations that affect simulation. The warning is caused by an incorrect timing model setting in the hard IP block for the `tl_cfg_sts` signals.

Affected Configurations

All IP Compiler for PCI Express hard IP variations that target an Arria II GZ device.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 11.0 of the IP Compiler for PCI Express.

PCI Express IP Core Cannot Negotiate to Gen 2 Data Rate on Some Devices

Auto negotiation to the Gen 2 data rate may fail in some devices. When this failure occurs, the PCI Express compiler is unable to switch to the Gen 2 data rate.

Affected Configurations

All PCI Express Gen 2 variations that target an Arria II GZ, Stratix IV GT, or Stratix IV GX device.

Workaround

No workaround exists for variations with transceivers configured to use the ATX PLL. You must configure the transceivers to use the CMU PLL.

To enable the IP core to negotiate to the Gen 2 data rate, generate a configuration that uses the CMU PLL. In versions 10.0 and 10.1, but not in version 11.0, you must then follow these steps:

1. After you generate the PCI Express compiler variations and before you compile the project, change directory to the location of the transceiver megafunction instance. The directory contains a *<variation>_serdes.v* or *<variation>_serdes.vhd* file, depending on the HDL.
2. Depending on the transceiver megafunction instance HDL, follow one of these steps:
 - If your transceiver megafunction instance is generated in Verilog HDL, type the following command:

```
qmegawiz -silent -wiz_override="enable_pcie_gen2_reset=true" \
        <variant>_serdes.v
```

- If your transceiver megafunction instance is generated in VHDL, type the following command:

```
qmegawiz -silent -wiz_override="enable_pcie_gen2_reset=true" \
        <variant>_serdes.vhd
```

Solution Status

This issue will be fixed in a future version of the IP Compiler for PCI Express.

Incorrect Arria II GZ Device Support in User Guide

Table 4-1 in the *PCI Express Compiler User Guide* incorrectly shows device support for Gen2 in Arria II GX devices and no Gen2 support in Arria II GZ devices. The opposite is true—Arria II GZ does support Gen2 and Arria II GX does not.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue is fixed in version 11.0 of the *IP Compiler for PCI Express User Guide*.

User Guide Incorrectly Includes an ALTGX Reset Signal

Figures 5-1 and 5-2 and Table 5-30 in the 10.1 release of the *PCI Express Compiler User Guide* include the `reset_reconfig_altgxb_reconfig` signal; however, this signal does not exist. In the 11.0 release of the *IP Compiler for PCI Express User Guide*, the signal remains in Figure 5-1.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue will be fixed in a future version of the *IP Compiler for PCI Express User Guide*.

Incorrect Numbering of 256-Bit Interface in User Guide

The bit ordering is reversed in Figure 5-24, Location of Headers and Data for Avalon-ST 256-Bit Interface, in the *PCI Express Compiler User Guide*. Bit 0 should be at the bottom of the figure and Bit 255 at the top.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue is fixed in version 11.0 of the *Stratix V Hard IP for PCI Express User Guide*. Starting in the Quartus II software release 11.0, the IP Compiler for PCI Express does not support Stratix V devices. Stratix V device support is now moved to the Stratix V Hard IP for PCI Express. The relevant figure in the new user guide is Figure 5-29.

User Guide Does Not Clarify that Posted Requests and Completions May Be Blocked if rx_st_mask Is Asserted

When the Application Layer asserts rx_st_mask to allow Posted Requests or Completions to bypass Non-Posted Requests in the PCIe hard IP RX Buffer, the Posted Requests and Completions may still be blocked by Non-Posted Configuration Space Requests. Asserting rx_st_mask does allow Posted Requests or Completions to bypass Non-Posted Memory Space or I/O Space requests that are routed to the Application Layer. As soon as a Non-Posted Configuration Space request (or a Non-Posted Memory or I/O space request that is being handled as an Unsupported Request) is encountered in the stream of requests in the RX Buffer while rx_st_mask is asserted, subsequent TLPs remain in the RX Buffer until all prior Non-Posted requests have been accepted by the Application Layer logic and rx_st_mask is deasserted.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express IP core in Arria II GX, Cyclone IV GX, and Stratix IV GX devices when the rx_st_mask is being used for performance enhancement or to block Non-Posted requests.

Workaround

Do not design your application layer logic so that `rx_st_mask` remains asserted until certain Posted Requests or Completions are received. As long as `rx_st_mask` is eventually deasserted without waiting for posted requests or completions, the blocking Non-Posted Configuration Requests will eventually complete.

Solution Status

This issue is documented in version 11.0 of the *IP Compiler for PCI Express User Guide*.

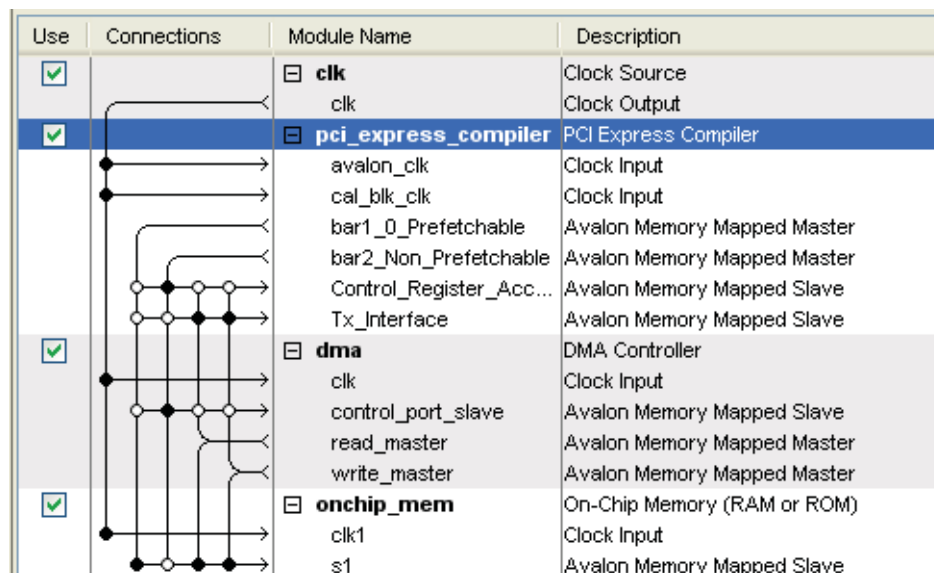
Incorrect Connections Shown in SOPC Builder Illustration

“Figure 16-3 Port Connections” in the *PCI Express Compiler User Guide* is missing a connection from the `dma_0 read_master` to the `onchip_memory2_0 s1`. In addition, it shows an incorrect connection from the `pcie_compiler_0 bar2_Non_Prefetchable` to `onchip_memory2_0 s1`.

Affected Configuration

This is a documentation error only. Figure 17-1 illustrates the correct connections.

Figure 17-1. System Port Connections



Workaround

No workaround is required. Make the connections described in Table 16-6, SOPC Builder Connections, in the *PCI Express Compiler User Guide*.

Solution Status

This issue is fixed in version 11.0 of the *IP Compiler for PCI Express User Guide*.

Memory Read Requests Hang in the SOPC Builder Soft IP Implementation

In SOPC Builder, the TX interface fails to forward read requests (MRd) to the data link layer due to incorrect decoding of the non-posted header credits.

Affected Configurations

This issue affects the soft IP implementation of the PCI Express IP core generated in SOPC Builder that uses the Avalon-MM interface to the application layer.

Workaround

The workaround is download the following solution:

http://www.altera.com/support/kdb/solutions/rd12062010_985.html.

Solution Status

This issue is fixed in version 10.1 SP1 of the PCI Express compiler.

Root Port Example Design Simulation Fails for Some Versions of ModelSim

Root port simulation fails using ModelSim versions 6.6c_1 for the Linux operating system (OS) or 6.6d for the Windows OS.

Affected Configurations

This issue affects root port example design simulations when using ModelSim 6.6c_1 for the Linux OS or 6.6d for the Windows OS in release 10.0 of the PCI Express Compiler.

Workaround

To prevent this failure, add the `-noimmedca` option to the `vsim` command in the `runtb.do` file.

Alternatively, you can update to version 10.1 of the PCI Express compiler.

Solution Status

This issue is fixed in version 10.1 of the PCI Express example design testbench.

VCS Simulation Script Fails for PCIe Root Port Design Example

The VCS simulation script, `runtb_vcs.sh`, does not work for PCI Express Design example described in the “*Testbench and Design Example*” chapter of the *PCI Express Compiler User Guide*.

Affected Configurations

This issue affects VCS simulation of the of the root port example.

Workaround

The workaround is to implement the changes described in the following solution:

http://www.altera.com/support/kdb/solutions/11022010_852.html.

A second alternative is to upgrade to version 10.1 of the Quartus II software.

Solution Status

This issue is fixed in version 10.1 of the PCI Express compiler.

SOPC Builder Hard IP Implementation Hangs when Entering L1 State

When the host programs the PMCSR register at address 0x1f to the D3 state, Hard IP endpoint variants created in SOPC Builder might hang while performing the power management message handshaking protocol with the root port.

Affected Configurations

This issue affects hard IP implementations of the PCI Express MegaCore function in SOPC Builder.

Workaround

The workaround is to set test_in[7] = 1 to disable all low state power negotiations.

Solution Status

This issue is fixed in version 10.1 of the PCI Express MegaCore function.

The Transceiver May Be Incorrectly Reset Leading to Unreliable Link Behavior

On rare occasions, the transceiver may be incorrectly reset leading to unreliable link behavior.

Affected Configurations

This issue affects the PCI Express MegaCore function targeting Stratix IV GX, Arria II GX, and Cyclone IV GX devices.

Workaround

Contact Altera Support for possible work arounds.

Solution Status

This issue is fixed in version 10.1 of the PCI Express MegaCore function.

Timing Analysis for Cyclone IV GX ×1 Variants

The Quartus II software does not perform timing analysis for the FPGA fabric in Cyclone IV GX ×1 variants; consequently, variants that would fail timing analysis are not identified.

Affected Configurations

This issue affects ×1 variants in the Cyclone IV GX device.

Workaround

You can manually create the required clock constraint. [Example 17-1](#) provides the equation for this constraint. In this equation *<n>* is 8.000 for a 125 MHz application clock and 16 for a 62.5 MHz application clock.

Example 17-1. Clock Constraint

```
# create_clock -name {core_clk_out} -period <n> -waveform { 0.000 8.000 } [get_nets
{*altpcie_hip_pipenlb_inst | core_clk_out~clkctrl}]
```

Solution Status

This issue is fixed in version 10.1 of the Quartus II software.

PCI Express Compliance Test Does Not Generate Gen2 Compliance Pattern

The PCI Express MegaCore function does not generate the Gen2 compliance pattern for the hard IP implementation in Stratix IV GX devices because the hard IP reset circuitry is holding the transceiver in reset.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function targeting Stratix IV GX devices that use reset scheme for *<variant>.v* or *.vhd* MegaCore function as described the “Reset and Clocks” chapter of the *PCI Express Compiler User Guide*. (It does not affect the *<variant>_plus.v* or *.vhd* MegaCore functions.)

Workaround

The workaround is to modify the definition of the rx_digitalreset_serdes signal in *<variant>.v* or *.vhd* file when running the compliance test. [Example 17-2](#) shows the required modification for compliance testing and the definition for normal operation.

Example 17-2. Definition of rx_digitalreset_serdes for Compliance Testing and Normal Operation

```
// Use this assignment for compliance testing
assign rx_digitalreset_serdes = rc_rx_digitalreset;
// Use this assignment for operation in non-compliance mode
assign rx_digitalreset_serdes = rc_rx_digitalreset | rst_rxpcs;
```

In addition, the reserved test_in bit (test_in[32]) must be defined as an input to the reset circuit to indicate that the DUT is performing the compliance test. When test_in[32] is set to 1, the portion of the reset circuit which introduces the compliance bug is bypassed. When this bit is set to 0, the PCI Express MegaCore function works in normal operating mode.

Solution Status

This issue is fixed in version 10.1 of the PCI Express MegaCore function.

Arria II GX Missing PLL_powerdown Signal when Using Custom Quartus II Installation

PCI Express MegaCore functions that target the Arria II GX device are missing the pll_powerdown signal which connects to the `<variation>_serdes.v` or `.vhd` module.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function targeting Arria II GX devices when using a custom Quartus II installation which does not include the Stratix IV device family.

Workaround

The workaround is to include the Stratix IV GX device family when you install the Quartus II software.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Compilation Fails for Hard IP PCI Express MegaCore Function in Stratix IV GT Devices

For designs that target Stratix IV GT devices in downbonded packages, the Quartus II software version 10.0 incorrectly places PCI Express hard IP block at the bottom transceiver block, which does not include the hard IP PCI Express MegaCore function. Compilation of the design fails with a message similar to the following:

```
Error: Can't assign I/O pad "<pad name>" to <pin name> because this causes failure in the placement of the other atoms in its associated channel.
```

```
Error: The transceiver block has no associated PCI Express hard IP block.
```

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function targeting Stratix IV GT devices.

Workaround

The workaround is to install version 10.0 SP1 of the Quartus II software.

Solution Status

This issue is fixed in version 10.0 SP1 of the Quartus II software.

PCI Express Hard IP Compilation Is Disabled for Gen1 x4 and x8 in Some Devices

The PCI Express Compiler v10.0 does not support IP and MegaWizard generation or regeneration of PCIe Gen1 x4 or x8 designs targeting the Stratix IV GX, Stratix IV GT, and HardCopy IV device families.

Affected Configurations

This issue affects Gen1 $\times 4$ or $\times 8$ designs targeting the hard IP implementation of the PCI Express MegaCore function in Stratix IV and HardCopy IV device families in the Quartus II 10.0 release.

Workaround

The workaround is to download and install Quartus II software patch described in the following solution.

http://www.altera.com/support/kdb/solutions/rd07012010_723.html.

A second alternative is to continue to use the Quartus II 9.1 SP2 release to generate the affected Gen1 PCI Express variant. After generating your variant using the Quartus II 9.1 SP2 software, you can compile your complete design using the either the 9.1 SP2 or 10.0 Quartus II 10.0 software release.

A third alternative is to parameterize the PCI Express MegaCore function to run at the Gen2 rate.

Solution Status

This issue is fixed in version 10.0 SP1 of the PCI Express MegaCore function.

PCI Express Design Example Does Always Not Close Timing in Stratix V GX and HardCopy IV GX in 250 MHz Modes

The PCI Express design example discussed in both the “*Getting Started*” and “*Testbench and Design Example*” chapters of the *PCI Express Compiler User Guide* does not always close timing in Stratix V GX and HardCopy IV GX devices running at 250 MHz.

Affected Configurations

This issue affects Stratix V GX and HardCopy IV GX devices running at 250 MHz in the Quartus II 10.0 release.

Workaround

There is no workaround.

Solution Status

This issue is fixed in version 10.0 SP1 of the PCI Express Compiler.

MSI Requests not Supported in Completer Only Mode

When you configure the PCI Express MegaCore function in **Completer Only** mode, if an MSI is sent by asserting an interrupt, any subsequent reads returns all zeros.

Affected Configuration

This issue affects variants that use the Avalon-MM interface and select **Completer Only** mode on the **Avalon Configuration** tab.

Workaround

Configure your MegaCore function in **Requester/Completer** mode.

Solution Status

This issue will be not fixed in a future version of the PCI Express MegaCore function.

Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Variation File

If you use PCI Express Compiler version 9.1 or later to edit a PCI Express Compiler variation that was created with Quartus II version 9.0 SP2 or earlier, a corrupted <variation>_serdes.v (or <variation>_serdes.vhd) file is created. This corrupt file leads to errors when trying to simulate or compile the PCI Express variation.

Affected Configurations

PCI Express variants created in Quartus II version 9.0 SP2 or earlier and edited in Quartus II release 9.1 or later.

Workaround

Before editing the variation with the newer PCI Express Compile version, delete the <variation>_serdes.v (or <variation>_serdes.vhd) file. If you had modified any settings in the SERDES file, re-enter them in PCI Express Compiler using the **Configure Transceiver Block** button on the **System Settings** tab.

Solution Status

This issue will not be fixed in a future version of PCI Express Compiler.

Revision History

Table 18–1 shows the revision history for the NCO MegaCore function.



For information about the new features, refer to the *NCO MegaCore Function User Guide*.

Table 18–1. NCO MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.

Errata

Table 18–2 shows the issues that affect the NCO MegaCore function v11.0, v10.1, and v10.0.



Not all issues affect all versions of the NCO MegaCore function.

Table 18–2. NCO MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	Mismatches Between Some Serial CORDIC MATLAB and RTL Models II	✓	—	—
	Warning Message Indicates Incorrect Support Level for Arria II GZ, Cyclone IV GX, HardCopy III, HardCopy IV E, and HardCopy IV GX Devices	✓	—	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—
15 Jul 10	Mismatches Between Some Serial CORDIC MATLAB and RTL Models I	✓	✓	✓
	Mismatches Between Some Small ROM MATLAB and RTL Models	✓	✓	✓
15 Mar 09	Warning Message Displayed Twice	✓	✓	✓
01 Oct 07	Mismatches Between Multiplier-Based MATLAB and RTL Models With Throughput One	✓	✓	✓

Mismatches Between Some Serial CORDIC MATLAB and RTL Models II

For the serial CORDIC architecture with **Phase Accumulator Precision** set to 25 and **Angular Resolution** set to 20, there can be mismatches between the outputs of the MATLAB model and the RTL.

Affected Configurations

Serial CORDIC architecture of the NCO MegaCore function with **Phase Accumulator Precision** set to 25 and **Angular Resolution** set to 20.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches.

Workaround

Set **Phase Accumulator Precision** or **Angular Resolution** to a different value, or use a different architecture.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Warning Message Indicates Incorrect Support Level for Arria II GZ, Cyclone IV GX, HardCopy III, HardCopy IV E, and HardCopy IV GX Devices

The NCO MegaCore function v11.0 provides final support for Arria II GZ and Cyclone IV GX devices, and HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices. However, when your NCO MegaCore function targets any of these device families, a warning message indicates support is only preliminary or HardCopy Companion. This warning message is erroneous.

Affected Configurations

All NCO MegaCore function variations that target an Arria II GZ, Cyclone IV GX, HardCopy III, HardCopy IV E, or HardCopy IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Compilation Targeting a Stratix V Device Fails

Designs that include an NCO IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

NCO IP core designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Mismatches Between Some Serial CORDIC MATLAB and RTL Models I

For the serial CORDIC architecture with **Phase Accumulator Precision** and **Angular Resolution** both set to values less than or equal to 10, there can be mismatches between the outputs of the MATLAB model and the RTL. These mismatches are due to rounding differences.

Affected Configurations

Serial CORDIC architecture of the NCO MegaCore function with **Phase Accumulator Precision** and **Angular Resolution** both set to values less than or equal to 10.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is only ± 1 .

Workaround

Set **Phase Accumulator Precision** and **Angular Resolution** to values greater than 10, or use a different architecture.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between Some Small ROM MATLAB and RTL Models

For the Small ROM architecture with a small **Angular Resolution** value and a large **Magnitude Precision** value, there can be mismatches between the outputs of the MATLAB model and the RTL. These mismatches are due to rounding differences.

Affected Configurations

Small ROM architecture of the NCO MegaCore function with a small **Angular Resolution** value and a large **Magnitude Precision** value.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is only ± 1 .

Workaround

To avoid this issue, modify your NCO MegaCore function in one of the following ways:

- Set **Angular Resolution** to a large value.
- Set **Magnitude Precision** to a small value.
- Use a different architecture.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Warning Message Displayed Twice

If you change the **Clock Rate** units to **mHz** in the **Parameter Setting** dialog box a warning message is displayed. After closing the warning message, if you then click on both the **Clock Rate** and the **Desired Output Frequency** boxes, two separate warning messages with the same content are displayed.

Affected Configurations

All configurations.

Design Impact

None.

Workaround

Close both of the warning messages.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between Multiplier-Based MATLAB and RTL Models With Throughput One

For the multiplier-based architecture with throughput = 1 (output every clock cycle), there can be mismatches between the outputs of the MATLAB model and the RTL design for values of magnitude precision. These mismatches seem to be rounding errors for very large values.

Affected Configurations

Multiplier-based architecture of the NCO MegaCore function with throughput = 1.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is small in both absolute and relative terms. For example, the MATLAB model calculates -536,870,910, whereas the RTL calculates -536,870,911.

Workaround

The RTL design works correctly, but comparison between the MATLAB model and the RTL cannot be done automatically.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Revision History

Table 19–1 shows the revision history for the Nios® II Processor MegaCore function.



For more information about the new features, refer to the *Nios II Processor Reference Handbook*. For information about new features and errata in the Nios II Embedded Design Suite, refer to the *Nios II Embedded Design Suite Release Notes and Errata*.

Table 19–1. Nios II Processor Revision History

Version	Date	Description
11.0	May 2011	Maintenance release
10.1	December 2010	Maintenance release
10.0	July 2010	Maintenance release

Errata

Table 19–2 shows the issues that affect the Nios II Processor versions 10.0 through 11.0.



Not all issues affect all versions of the Nios II Processor.

Table 19–2. Nios II Processor Errata

Added or Updated	Issue	Affected Version			
		11.0	10.1 SP1	10.1	10.0
15 Jan 11	Cannot Remove EIC Interface from Nios II Processor	Fixed	✓	✓	✓
	Error: Debug Slave <slave interface name> Not Connected to data_master	—	Fixed	✓	—
15 Dec 10	The cpu_resetrequest and cpu_resettaken Signals Do Not Export	Fixed	✓	✓	—
	Custom Instruction Import Fails and Freezes GUI	—	—	Fixed	✓
15 Jul 10	Error Running Nios II Project: 'Downloading ELF Process failed'	✓	✓	✓	✓
15 Nov 09	Design Assistant Error on Clock Signal Source in HardCopy Designs	—	—	—	Fixed
	Nios II Ports Created Incorrectly	✓	✓	✓	✓
15 Oct 07	Errors Adding Custom Instruction to the Nios II Processor	✓	✓	✓	✓

Cannot Remove EIC Interface from Nios II Processor

In SOPC Builder, if you configure a Nios II/f processor core with the external interrupt controller (EIC) interface, then change the core to a Nios II/s or Nios II/e, the EIC interface remains. The Nios II/s and Nios II/e cores do not support the EIC. As a result, the following error message appears:

```
Error: cpu_0.interrupt_controller_in: "cpu_0.interrupt_controller_in"
must be connected to an Avalon-ST source
```

On the **Advanced Features** tab, the **Interrupt Controller** parameter is disabled and you cannot change from the EIC to the internal interrupt controller.

Affected Configurations

Nios II/s and Nios II/e processor cores

Workaround

To correct this condition, perform the following steps:

1. Change the processor core back to Nios II/f.
2. In the **Advanced Features** tab, select **Internal** to remove the EIC interface and revert to the internal interrupt controller.
3. Change the processor back to the desired core, Nios II/s or Nios II/e.

Solution Status

This issue is fixed in the Nios II processor version 11.0.

Error: Debug Slave <slave interface name> Not Connected to data_master

In Qsys, for designs that have Nios II processors with tightly-coupled instruction masters and nontightly-coupled data masters, you might receive the following message:

```
Debug slave <slave_interface_name> not connected to data_master.
```

Affected Configurations

This issue affects all designs that use Nios II processor in Qsys, which has tightly-coupled instruction masters and nontightly-coupled data masters.

Design Impact

There is no design impact.

Workaround

Use SOPC Builder rather than Qsys.

Alternatively, upgrade to v10.1 SP1 or later.

Solution Status

Fixed in v10.1 SP1

The `cpu_resetrequest` and `cpu_resettaken` Signals Do Not Export

If you wish to include the `cpu_resetrequest` and `cpu_resettaken` signals for the Nios II processor, these signals do not appear on the top-level Qsys system.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact

Workaround

Use SOPC Builder rather than Qsys.

Solution Status

This issue is fixed in the Nios II processor version 11.0.

Custom Instruction Import Fails and Freezes GUI

If you click the **Import** button on the **Custom Instructions** tab in the Nios II MegaWizard interface, the GUI freezes.

Workaround

There is currently no workaround for this problem.

Solution Status

This issue is fixed in the Nios II processor version 10.1.

Error Running Nios II Project: 'Downloading ELF Process failed'

If the Nios II processor's `cpu.data_master` port is not connected to all program memories (memories to which the `.elf` file is downloaded) the software project fails to run on Nios II hardware.

Failure to connect `cpu.data_master` to all program memories is a design error that the Nios II Software Build Tools (SBT) does not detect.

Affected Configurations

Any Nios II system whose data masters are not correctly set up as described in the previous section

Design Impact

You cannot download software to the program memories.

Workaround

Connect `cpu.data_master` to all program memories.

Solution Status

Not fixed

Design Assistant Error on Clock Signal Source in HardCopy Designs

When you run the Quartus® II Design Assistant on a HardCopy III or HardCopy IV design, the following error message might appear:

```
Rule C106: Clock signal source should not drive registers that are \
          triggered by different clock edges ; clk ;
```

This error occurs if your HardCopy III or HardCopy IV design incorporates a Nios II/s processor core with a logic element (LE)-based multiplier. Only Stratix® designs can be converted for HardCopy III or HardCopy IV devices. In a Stratix design, it is preferable to implement the multiplier in a DSP block, which provides better performance than an LE-based multiplier.

Affected Configurations

HardCopy III and HardCopy IV designs incorporating the Nios II/s processor core with an LE-based multiplier.

Design Impact

You cannot compile a HardCopy III or HardCopy IV design incorporating the Nios II/s processor core with an LE-based multiplier.

Workaround

Implement the Nios II multiplier with DSP blocks when targeting a HardCopy III or HardCopy IV device.

Solution Status

Fixed in v. 10.0

Nios II Ports Created Incorrectly

A threading issue between SOPC Builder and the Nios II MegaWizard™ interface occasionally causes HDL file analysis to fail. This creates all ports as std_logic input with width 1.

Affected Configurations

Nios II processor systems with custom instructions.

Design Impact

Design fails to run in ModelSim®.

Workaround

After adding your custom instruction, close and relaunch SOPC Builder.

Solution Status

Not fixed

Errors Adding Custom Instruction to the Nios II Processor

You might get spurious errors after adding custom instruction slave ports through the Nios II MegaWizard interface.

Affected Configurations

Any Nios II system featuring custom instructions.

Design Impact

No design impact. The error messages are benign.

Workaround

Save your system in SOPC Builder. Close and then relaunch SOPC Builder.

Solution Status

Not fixed

Revision History

Table 20–1 shows the revision history for the PCI Compiler.


 For more information about the new features, refer to the *PCI Compiler User Guide*.

Table 20–1. PCI Compiler Revision History

Version	Date	Description
11.0	May 2011	Final support for Arria II GZ, Cyclone III LS, Cyclone IV E, and Cyclone IV GX device.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> ■ Preliminary support for Arria II GZ devices. ■ Final support for Arria II GX and Stratix IV GT devices.
10.0	July 2010	Maintenance release.

Errata

Table 20–2 shows the issues that affect the PCI Compiler v11.0, v10.1, and v10.0.


 Not all issues affect all versions of the PCI Compiler.

Table 20–2. PCI Compiler MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
01 Apr 10	Configuration Write to Invalid Address Repeats Continuously	✓	✓	✓
15 Nov 09	Designs With Cyclone III LS Devices Fail to Meet Timing	✓	✓	✓
15 May 09	F1152 Packages for HardCopy III and HardCopy IV-E Not Supported	✓	✓	✓
	Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported	✓	✓	✓
01 Nov 08	Designs With Stratix IV Devices Fail to Meet Timing	✓	✓	✓

Configuration Write to Invalid Address Repeats Continuously

A configuration write to an invalid configuration space address causes PCI Compiler to attempt continuous writes, and prevents further PCI reads or writes.

Affected Configuration

All PCI Compiler configurations.

Design Impact

The PCI Compiler continuously repeats the configuration write and does not proceed to the next operation.

Workaround

Make sure that you do not write to an invalid configuration space address.

Solution Status

This issue will not be fixed.

Designs With Cyclone III LS Devices Fail to Meet Timing

Timing fails when using Cyclone III LS devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Cyclone III LS device family with C8 speed grade, and all PCI Compiler designs targeting the EP3CLS150 or EP3CLS200 devices with C7 speed grade.

Design Impact

The PCI Compiler designs with some Cyclone III LS devices may not meet timing requirements.

Workaround

None.

Solution Status

This issue will not be fixed.

F1152 Packages for HardCopy III and HardCopy IV-E Not Supported

PCI Compiler does not support F1152 packages for HardCopy III and HardCopy IV-E.

Affected Configuration

All PCI Compiler configurations using the F1152 packages for HardCopy III and HardCopy IV-E.

Design Impact

The PCI Compiler designs with F1152 packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the PCI Compiler.

Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported

PCI Compiler does not support wirebond packages for HardCopy III and HardCopy IV-E.

Affected Configuration

All PCI Compiler configurations using the wirebond packages for HardCopy III and HardCopy IV-E.

Design Impact

The PCI Compiler designs with wirebond packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the PCI Compiler.

Designs With Stratix IV Devices Fail to Meet Timing

Timing fails when using Stratix IV devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Stratix IV devices with the slowest speed grade, C4.

Design Impact

The PCI Compiler designs with some Stratix IV devices may fail to meet timing.

Workaround

None.

Solution Status

This issue will not be fixed.

Revision History

Table 21–1 shows the revision history for the POS-PHY Level 4 MegaCore function.



For more information about the new features, refer to the *POS-PHY Level 4 MegaCore Function User Guide*.

Table 21–1. POS-PHY Level 4 MegaCore Function Revision History

Date	Version	Description
May 2011	11.0	Maintenance release.
December 2010	10.1	Maintenance release.
July 2010	10.0	Maintenance release.

Errata

The following sections addresses known errata and documentation issues for the POS-PHY Level 4 MegaCore function. Errata are functional defects or errors, which may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 21–2 shows the issues that affect the POS-PHY Level 4 MegaCore function v11.0, v10.1, and v10.0.



Not all issues affect all versions of the POS-PHY Level MegaCore function.

Table 21–2. POS-PHY Level 4 MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	VHDL IP Functional Simulation Fails	✓	—	—
15 Mar 11	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—
15 Dec 10	Import PLL Frequency Launches Incorrect Parameter Editor	✓	✓	—
15 Sep 10	Cannot Edit ALTPLL Megafunction for Stratix V Devices	✓	✓	✓
15 Jul 10	Incorrect LVDS Frequencies in Quartus II Compilation	✓	✓	✓
15 May 08	Errors when Editing Transmitters v7.2 or Earlier in v8.0	✓	✓	✓
	Training Interval is Greater than Specified	✓	✓	✓

Table 21–2. POS-PHY Level 4 MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
01 May 07	Irrelevant Signals: err_ry_msop* & err_ry_meop*	✓	✓	✓
	Warning Message: Pin “err_rd_dpa” Stuck at GND	✓	✓	✓
	IP Toolbench Error After Changing the Device Family	✓	✓	✓
	IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices	✓	✓	✓
	IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted	✓	✓	✓

VHDL IP Functional Simulation Fails

When running the demonstration testbench with VHDL simulations, you receive the following error:

```
Signal "wire_gnd" is type ieee.std_logic_1164.std_logic; expecting type
ieee.std_logic_1164.std_logic_vector.
```

Affected Configurations

This issue affects Stratix V receiver variants.

Design Impact

There is no design impact.

Workaround

Use Verilog HDL simulations.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Compilation Targeting a Stratix V Device Fails

Designs that include a POS-PHY Level 4 IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

POS-PHY Level 4 IP cores that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.

2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in the Quartus II software version 11.0.

Import PLL Frequency Launches Incorrect Parameter Editor

If you click **Import PLL Frequency**, the ALTLVDS_TX parameter editor correctly starts, but you can incorrectly edit all parameters not just the **Frequency /PLL Settings** page parameters.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

To work around this issue, when the ALTLVDS_TX parameter editor starts on the **General parameters** page, follow these steps:

1. Click **Next** to go to the **Frequency/PLL Settings** page.
2. Select desired input clock rate.
3. Click **Finish** twice to skip the remaining pages and close the ALTLVDS_TX parameter editor.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Cannot Edit ALTPLL Megafunction for Stratix V Devices

You cannot edit the ALTPLL megafunction with the parameter editor.

Affected Configurations

This issue affects variations for Stratix V devices.

Design Impact

There is no design impact.

Workaround

To work around this issue, manually modify the ALTPLL variation to the desired parameters. The only parameter that generally requires modification is the phase shift, which is currently set to a quarter clock period.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Incorrect LVDS Frequencies in Quartus II Compilation

For most of the data rates, the LVDS frequencies, which the Quartus II software reports after compilation in the Timequest Timing Analyzer under the **Clocks** section, are incorrect. Though, for some data rates (800 Mbps, 1000 Mbps, 1250 Mbps), the calculated frequencies are correct

Affected Configurations

This issue affects 64 and 128 bit RX and TX variations for Stratix V devices.

Design Impact

The Quartus II software uses incorrect clock frequencies during compilation.

Workaround

To work around this issue, use only the 800-Mbps, 1,000-Mbps or 1,250-Mbps data rates.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Errors when Editing Transmitters v7.2 or Earlier in v8.0

If you edit a v7.2 or earlier 64 or 128-bit transmitter MegaCore variation in the v8.0 or later MegaWizard Plug-In, the PLL input frequency is set to 1 MHz, which is incorrect.

Affected Configurations

This issue affects 64- and 128-bit transmitters.

Design Impact

There is no design impact.

Workaround

To work around the issue, follow these steps:

1. Click in the **LVDS Data Rate** dialog box.
2. Press **Enter**.

The PLL input frequency parameter resets to the correct value—data rate divided by deserialization factor.

Solution Status

This issue will never be fixed.

Training Interval is Greater than Specified

In corner cases, for example with datapath is 256 and a high number of ports and low burst length (BURSTLEN), the maximum training interval (MaxT) is greater than you specify.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

Add (or subtract) another BURSTLEN to calculation, so MaxT is $SET_MaxT + 2 \times BURSTLEN$.

Solution Status

This issue will never be fixed.

Irrelevant Signals: err_ry_msop* & err_ry_meop*

After generation, the MegaCore function may include the following irrelevant output signals, which you can safely ignore:

- err_ry_msop*
- err_ry_meop*

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Warning Message: Pin “err_rd_dpa” Stuck at GND

During compilation, the Quartus II software issues the following warning, which you can safely ignore:

```
Pin "err_rd_dpa" Stuck at GND
```

Affected Configurations

This issue affects all non-Stratix GX receivers with dynamic phase alignment (DPA) enabled.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

The Calendar Length Value Cannot Equal 256

If the transmitter’s status interpretation mode is set to pessimistic, the programmable calendar length support parameter must be less than the maximum number of ports (< 256), unless the asymmetric port support parameter is enabled.

Affected Configurations

This issue affects all transmitter variations of the MegaCore function that use the pessimistic mode for status interpretation, and that do not have the asymmetric port support parameter enabled.

Design Impact

The status first-in first-out (FIFO) buffer may lock up. The scheduler in individual buffers variations of the MegaCore function may also lock up.

Workaround

If you turn on the programmable calendar length support in your variation, make sure that you set the calendar length value—via a pin or the Avalon Memory-Mapped (Avalon-MM) register—to less than the maximum calendar length (that is, 256); unless asymmetric port support is enabled, in which case you select the maximum calendar length in IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Error After Changing the Device Family

If you change the device family when editing an existing custom megafunction variation (POS-PHY Level 4 MegaCore function variation) without first changing the device family in the Quartus II project, an error may occur when generating the MegaCore function. This results in a MegaCore function generation error message.

This issue also applies when creating a new custom megafunction variation, if you use a different device family to that specified in the Quartus II project.

Affected Configurations

This issue can affect all configurations.

Design Impact

You may not be able to generate a MegaCore function.

Workaround

Before using the MegaWizard Plug-In Manager to create or edit a POS-PHY Level 4 custom megafunction variation, make sure that a Quartus II project exists and that the required device family is set in the project. To set the device family, in the Quartus II software, on the Assignments menu click **Device**.

When using the MegaWizard Plug-In Manager to create or edit the megafunction variation, set the device family to be the same as the device family set in the Quartus II project. You can set the device family in the **Basic Parameters** tab when parameterizing the MegaCore function.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices

If you select **HardCopy Stratix** in the MegaWizard Plug-In Manager and you turn on **Generate Simulation Model** and generate a MegaCore function variation, IP Toolbench fails with an error.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot generate an IP functional simulation model.

Workaround

Select the Stratix family in the MegaWizard Plug-In Manager.

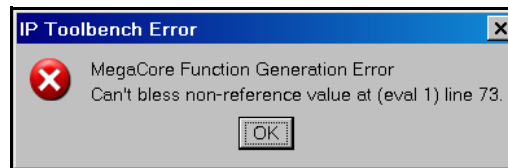
Solution Status

This issue will never be fixed.

IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted

By clicking the IP Toolbench **Generate** button, you start generating a POS-PHY Level 4 MegaCore function variation. If, during generation, you click the **Cancel** button (Generation window) and click the IP Toolbench **Generate** button again to restart the generation, IP Toolbench fails and produces the following error message:

Figure 21-1. IP Toolbench Generation Error Message



Affected Configurations

This issue affects all variations of the MegaCore function.

Design Impact

IP Toolbench does not generate any files.

Workaround

To cancel a generation and avoid this error, follow these steps:

1. Click the **Cancel** button in the Generation window.
2. Close IP Toolbench by clicking the **x** in the upper right corner.
3. Relaunch IP Toolbench from the MegaWizard Plug-In Manager (Tools menu).



Refer to the Getting Started chapter of the *POS-PHY Level 4 MegaCore Function User Guide* for instructions on using IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Revision History

Table 22–1 shows the revision history for the QDRII SRAM MegaCore function.



For more information about the new features, refer to the [QDRII SRAM MegaCore Function User Guide](#).

Table 22–1. QDRII SRAM MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	Maintenance release.
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.

Errata

Table 22–2 shows the issues that affect the QDRII SRAM MegaCore functionv11.0, 10.1, and 10.0.



Not all issues affect all versions of the QDRII SRAM MegaCore function.

Table 22–2. QDRII SRAM MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 08	Termination Error When Compiling Design	✓	✓	✓
01 Dec 06	Incorrect IP Toolbench Latency Behavior	✓	✓	✓
01 Nov 06	Simulating with the VCS Simulator	✓	✓	✓
	TimeQuest Timing Analyzer Failure	✓	✓	✓
	PLL Placement	✓	✓	✓
01 Nov 05	Constraints Errors With Companion Devices	✓	✓	✓
	Supported Device Families	✓	✓	✓
	Compilation Error (Stratix II Series & HardCopy II Devices Only)	✓	✓	✓
	Gate-Level Simulation Filenames	✓	✓	✓
	The ModelSim Simulation Script Does Not Support Companion Devices	✓	✓	✓

Termination Error When Compiling Design

The Fitter reports the following error: "Error Bidirectional I/O "cq" uses the parallel termination but does not have dynamic termination control."

Affected Configurations

This issue affects designs using the QDRII SRAM Controller.

Design Impact

The design fails to fit.

Workaround

At top-level design, change the pin direction from inout to input for
- qdr_ii_cq_<index>; qdr_ii_cqn_<index>.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Incorrect IP Toolbench Latency Behavior

When you open the IP Toolbench Parameterize window, you can select any latency for the default QDRII, but it only supports 1.5.

Affected Configurations

This issue affects all QDRII SRAM configurations.

Design Impact

IP Toolbench does not generate a variation and gives the following error message:

```
MegaCore Function Generation Error
IP Functional Simulation creation Failed. The following error was
returned:
Error: Top-level design entity
"qdr_auk_qdr_ii_sram_avalon_controller_ipfs_wrap" is undefined.
```

Workaround

For longer latency, select QDRII+.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Simulating with the VCS Simulator

The QDRII SRAM Controller MegaCore function does not support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

There is no workaround for VHDL simulations. For Verilog HDL simulations. Change line 154 in the `qdrii_model.v` file to:

```
begin : f1
```

Also, change line 417 to:

```
begin : f2
```

Solution Status

This issue will not be fixed.

TimeQuest Timing Analyzer Failure

When you use the Quartus II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest timing analyzer.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

PLL Placement

The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to fail hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins; otherwise, the source synchronous compensation does not compensate for the expected delays.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails hold timing analysis.

Workaround

The PLL must be located on the same side of the device as the CQ/CQn groups, for the PLL to compensate properly.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Constraints Errors With Companion Devices

When you change the device in your project or add a HardCopy II companion device to a Stratix II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails.

Workaround

Reassign the byte groups for the new device in the constraints editor.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Supported Device Families

The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot compile a design.

Workaround

Ensure you choose a supported device family for the Quartus II project.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Compilation Error (Stratix II Series & HardCopy II Devices Only)

The IP Toolbench Constraints window allows the illegal situation where you can share DQ groups on the top and bottom banks for Stratix II series and HardCopy devices. When you compile your design the Quartus II software issues a no fit error.

Affected Configurations

This issue affects all DQS mode QDRII SRAM controllers on Stratix II series and HardCopy II devices.

Design Impact

When you choose **Start Compilation**, there is an error message and the design does not compile.

Workaround

If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytgroups on either the top or the bottom of the device, but not both.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects *<project name>.vho* or *.vo* and *<project name>_v* or *_vhd.sdo* files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename *<filename>.vho* file to *<project name>.vho*.
2. Rename *<filename>.sdo* file to *<project name>_vhd.sdo*.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the *<filename>.vo* file to *<project name>.vo*.
2. Rename the *<filename>.sdo* file to *<project name>_v.sdo*.

3. In the `<project name>.vo` file change the following line to point to the `<project name>_v.sdo` file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

The ModelSim Simulation Script Does Not Support Companion Devices

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

Affected Configurations

This issue affects designs with companion devices.

Design Impact

The simulation script does not run.

Workaround

Edit the ModelSim script to include the correct libraries.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Revision History

Table 23–1 shows the revision history for the QDR II and QDR II+ SRAM Controller with UniPHY.



For more information about the new features, refer to the *QDR II and QDR II+ SRAM Controller with UniPHY User Guide*.

Table 23–1. QDR II and QDR II+ SRAM Controller with UniPHY Revision History

Date	Version	Description
July 2011	11.0 SP1	Maintenance release
May 2011	11.0	<ul style="list-style-type: none"> Added Nios II-based sequencer Upgraded f_{MAX} (with Nios II sequencer) to 550 MHz for Stratix III, Stratix IV, and Stratix V devices
December 2010	10.1	<ul style="list-style-type: none"> Added preliminary support for Arria II GZ and Stratix V Added new generated directory structure Added new OCT Sharing Interface feature Added External Memory Interface Toolkit
September 2010	10.0 SP1	Maintenance release
July 2010	10.0	<ul style="list-style-type: none"> Final support for Arria II GX devices Added width expansion feature Added variable latency feature

Errata

Table 23–2 shows the issues that affect the QDR II and QDR II+ SRAM Controller with UniPHY v11.0, 10.1, and 10.0.



Not all issues affect all versions of the QDR II and QDR II+ SRAM Controller with UniPHY.

Table 23–2. QDR II and QDR II+ SRAM Controller with UniPHY Errata (Part 1 of 3)

Added or Updated	Issue	Affected Version				
		11.0 SP1	11.0	10.1	10.0 SP1	10.0
15 Jul 11	Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations	✓	—	—	—	—
	Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error	✓	—	—	—	—

Table 23-2. QDR II and QDR II+ SRAM Controller with UniPHY Errata (Part 2 of 3)

Added or Updated	Issue	Affected Version				
		11.0 SP1	11.0	10.1	10.0 SP1	10.0
1 Jul 11	VHDL-Generated Fileset Can Encounter Synthesis Problems	✓	✓	—	—	—
	UniPHY CSR Ports Not Functioning Correctly	Fixed	✓	—	—	—
	Stratix V Memory Interfaces May Exhibit Write Timing Failure	✓	✓	—	—	—
	UniPHY IP Generation Fails if Quartus II Path Contains a Space	✓	✓	—	—	—
	Example Project Fails to Simulate When HardCopy Compatibility Enabled	✓	✓	—	—	—
	NativeLink RTL Simulation May Fail	Fixed	✓	—	—	—
	Error Messages in ModelSim Flow for Eclipse	✓	✓	—	—	—
	ModelSim Waveform Viewer Shows Only clk and reset Signals	Fixed	✓	—	—	—
	PLL Master Required for Simulation of PLL Slave	✓	✓	—	—	—
	Minimum Pulse Width Timing Failure	Fixed	✓	—	—	—
	Write Timing Violation at 550MHz	Fixed	✓	—	—	—
	Simulation Fails with “Undefined System Task Call” Error	✓	✓	—	—	—
	Unable to Directly Recompile 10.1 Design in 11.0	✓	✓	—	—	—
	Using UniPHY-based Memory IP with SOPC Builder	✓	✓	—	—	—
	Using Avalon-MM Traffic Generator and BIST Engine	✓	✓	—	—	—
	Simulation Fails when Generating VHDL for Designs Using Nios II-based Sequencer	✓	✓	—	—	—
	Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys	✓	✓	—	—	—
	Conduit Error Messages Displayed in Qsys	✓	✓	—	—	—
	Example Design Simulation May Fail in NC Sim	✓	✓	—	—	—
	Example Design Can Fail For Certain Parameterizations	✓	✓	—	—	—
	Simulation of Example Designs Can Fail or Produce Warnings	✓	✓	—	—	—
	Compilation of a UniPHY Example Design Can Produce Warnings	✓	✓	—	—	—
15 Mar 11	VHDL-only Simulation Not Supported	—	Fixed	✓	—	—
15 Dec 10	NativeLink Simulation fails for VHDL Output	✓	✓	✓	—	—
	NativeLink Simulation fails for VHDL Output	—	—	—	✓	✓
	Timing-related Warning Messages When Sharing PLLs on Stratix V Devices	✓	✓	✓	—	—
	Reset Synchronizer May Cause Design to Fail Timing	✓	✓	✓	—	—
	Compilation Fails if Synthesis Fileset is Mixed with Example Project Files	—	Fixed	✓	—	—
	Warning Messages Displayed When Compiling for Stratix V Devices	—	✓	✓	—	—
	Cannot Launch MegaWizard Plug-In Manager by Opening Example Design	✓	✓	✓	—	—
	Example Design May Not Compile for IP Cores from Earlier Versions	—	Fixed	✓	—	—
	Calibration Failure in Earlier Versions	—	Fixed	✓	—	—
	SOPC Builder-generated Systems Cannot Serve as Top-Level Design	—	Fixed	✓	—	—
	Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices	✓	✓	✓	—	—
15 Sept 10	Simulation Fails—PLL Clocks Out of Synchronization	✓	✓	✓	✓	✓

Table 23–2. QDR II and QDR II+ SRAM Controller with UniPHY Errata (Part 3 of 3)

Added or Updated	Issue	Affected Version				
		11.0 SP1	11.0	10.1	10.0 SP1	10.0
15 Aug 10	Selecting VHDL Gives a Verilog HDL IP Core	✓	✓	✓	✓	✓
15 Jul 10	BSF File Not Generated	—	—	Fixed	✓	✓
	Global Signal Assignments Not Applied	✓	✓	✓	✓	✓
	Simulation Error	—	—	—	Fixed	✓
	Incorrect Clock Uncertainty	—	Fixed	✓	✓	✓
	IP Core May Not Operate Below 167MHz	—	Fixed	✓	✓	✓
15 Nov 09	UniPHY DQS Clock Buffer Location	✓	✓	✓	✓	✓
	IP Functional Simulation Model	✓	✓	✓	✓	✓
	No Link to User Guide from Wizard	✓	✓	✓	✓	✓
	QDR II SRAM Emulated Mode	✓	✓	✓	✓	✓

Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations

Designs containing both UniPHY and ALTMEMPHY instantiations may encounter erroneous clock failures during timing analysis.

Affected configurations

This issue affects all configurations containing both UniPHY and ALTMEMPHY instantiations.

Design Impact

Timing analysis may incorrectly report that some paths are failing timing.

Workaround

The workaround for this issue is to open the UniPHY `<core_name>_report_timing.tcl` and `<core_name>_pin_map.tcl` files in an editor, and make the following change in each file:

Locate the `traverse_to_ddio_out_pll_clock` function name, and append the numeral 2 to the function name, making it `traverse_to_ddio_out_pll_clock2`.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error

Simulation with NC Sim or Riviera-PRO may fail with the error message:
Unsupported memory slice specification using part select or indexed part select.

Affected configurations

This issue affects all configurations using the Nios II-based sequencer.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to open the `sequencer_scc_mgr.sv` file in an editor, and locate the following code:

```
integer unsigned setting_offsets[1:9];
t_setting_mask setting_masks [1:9];

generate
    if (FAMILY == "STRATIXV")
    begin
        assign setting_offsets[1:9] = '{ 'd0, 'd12, 'd17, 'd25, 'd30, 'd36, 'd0,
        'd6, 'd12 };
        assign setting_masks [1:9] = '{ 'b011111111111, 'b011111,
        'b011111111, 'b011111, 'b0111111, 'b0111111, 'b0111111,
        'b011111111111 };
    end
    else
    begin
        assign setting_offsets[1:9] = '{ 'd0, 'd4, 'd8, 'd12, 'd17,
        'd21, 'd0, 'd4, 'd7 };
        assign setting_masks [1:9] = '{ 'b01111, 'b01111, 'b01111,
        'b11111, 'b01111, 'b00111, 'b01111, 'b00111, 'b01111 };
    end
endgenerate
```

For Stratix V devices, replace the preceding code with the following:

```
integer setting_offsets[1:9] = '{ 'd0, 'd12, 'd16, 'd24, 'd27, 'd33, 'd0,
'd6, 'd12 };
t_setting_mask setting_masks [1:9] = '{ 'b011111111111, 'b01111,
'b011111111, 'b0111, 'b0111111, 'b0111111, 'b0111111,
'b011111111111 };"
```

For non-Stratix V device families, replace the code with the following:

```
integer setting_offsets[1:9] = '{ 'd0, 'd4, 'd8, 'd12, 'd17, 'd21, 'd0,
'd4, 'd7 };
t_setting_mask setting_masks [1:9] = '{ 'b01111, 'b01111, 'b01111, 'b11111,
'b01111, 'b00111, 'b01111, 'b00111, 'b01111 };
```


Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

VHDL-Generated Fileset Can Encounter Synthesis Problems

An error in the VHDL-generated wrapper for the synthesis fileset can result in a variety of synthesis problems.

Affected configurations

This issue affects all configurations using VHDL.

Design Impact

Synthesis problems can result.

Workaround

The workaround for this issue is to open the generated wrapper file in a text editor, and replace all ports of the form `std_logic_vector(0 downto 0)` with `std_logic`.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

UniPHY CSR Ports Not Functioning Correctly

The CSR ports in UniPHY-based interfaces do not function correctly.

Affected configurations

This issue affects all configurations using CSR ports.

Design Impact

The CSR ports do not function correctly.

Workaround

There is no workaround for this issue. Consider using the JTAG Avalon master interface instead.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Stratix V Memory Interfaces May Exhibit Write Timing Failure

Memory interfaces targeting Stratix V devices may exhibit write setup or write hold timing failures.

Affected configurations

This issue affects configurations targeting Stratix V devices.

Design Impact

Write setup or write hold timing failures occur.

Workaround

A workaround for interfaces running at 400MHz or slower is to enable the high-performance Nios II-based sequencer instead of the RTL-based sequencer.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

UniPHY IP Generation Fails if Quartus II Path Contains a Space

UniPHY IP generation fails if the installation path of the Quartus II software contains one or more spaces.

Affected configurations

This issue affects all configurations.

Design Impact

UniPHY IP generation fails.

Workaround

The workaround for this issue is to ensure that the Quartus II installation path contains no spaces.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Example Project Fails to Simulate When HardCopy Compatibility Enabled

The example project for designs generated with **HardCopy Compatibility Mode** enabled can fail to simulate.

Affected configurations

This issue affects QDR II and QDR II+ UniPHY designs generated with **HardCopy Compatibility Mode** enabled.

Design Impact

The example project fails in simulation.

Workaround

The workaround for this issue is to modify two files, as follows:

1. In a text editor, open the file
`<variant_name>_example_design/simulation/<variant_name>_example_sim/
submodules/<variant_name>_example_sim_<variant_name>_example_sim.v`
2. In the above file, change the line
`.INIT_FILE = ("dut_dut_e0_if0_p0_sequencer_rom.v")`
to
`.INIT_FILE =
("<variant_name>_example_sim_<variant_name>_example_sim_e0_if0_p0_
sequencer_rom.v")`
3. In a text editor, open the file
`<variant_name>_example_design/simulation/<variant_name>_example_sim.qsf`
4. In the above file, add the following lines:
`set_global_assignment -name EDA_TEST_BENCH_FILE
<variant_name>_example_sim/submodules/hc_rom_reconfig_gen.sv -
section_id uniphy_rtl_simulation -hdl_version SystemVerilog_2005`

and

`set_global_assignment -name SOURCE_FILE
<variant_name>_example_sim/submodules/<variant_name>_example_sim_
<variant_name>_example_sim_e0_if0_p0_sequencer_rom.hex`

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

NativeLink RTL Simulation May Fail

NativeLink RTL simulation may fail and report warnings that a file could not be opened for reading.

Affected configurations

This issue affects all UniPHY protocols.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to edit the project's `.qsf` settings file and add to it all the `.hex` and `.mif` files residing in the directory:

```
<variant_name>_example_design/simulation/<variant_name>_example_sim/  
submodules/
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Error Messages in ModelSim Flow for Eclipse

Designs generated with the **Enable support for Nios II ModelSim flow in Eclipse** option enabled can produce error messages reporting attempts to read from uninitialized data locations.

Affected configurations

This issue affects QDR II and QDR II+ designs generated with the **Enable support for Nios II ModelSim flow in Eclipse** option enabled.

Design Impact

Error messages are displayed.

Workaround

There is no workaround for this issue; you may ignore the error messages.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

ModelSim Waveform Viewer Shows Only clk and reset Signals

ModelSim simulation of the example design for MegaWizard-generated systems displays only the clk and reset signals in the waveform viewer.

Affected configurations

This issue affects all MegaWizard-generated QDR II and QDR II+ SRAM Controller with UniPHY interfaces.

Design Impact

Only clk and reset waveforms are displayed.

Workaround

The workaround for this issue is as follows:

1. Open the existing
`<variant_name>_example_design/simulation/<variant_name>_example_sim.qsf`
file in a text editor and add the following line to the file:

```
set_global_assignment -name EDA_NATIVELINK_SIMULATION_SETUP_SCRIPT
my_wave.do -section_id eda_simulation
```

Where `<my_wave>.do` is a file name of your choice.

2. Create a ModelSim `<my_wave>.do` file in the
`<variant_name>_example_design/simulation` directory.

Ensure that the `<my_wave>.do` file has the following content:

```
"
add wave dut/<variant_name>_example_sim_inst/*
run -all
"
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

PLL Master Required for Simulation of PLL Slave

The example simulation design (generated in the
`<variation_name>_example_design\simulation` folder) does not function correctly if the core is parameterized with **PLL Sharing Mode = Slave**, **DLL Sharing Mode = Slave**, or **OCT Sharing Mode = Slave**.

Affected configurations

This issue affects all protocols with UniPHY interfaces employing slave PLLs, DLLs, or OCTs.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to ensure that a master instantiation is provided to drive the slave. To do this, follow these steps (a PLL example is shown):

1. Generate a second, identically parameterized, IP core with **PLL Sharing Mode** set to **Master**.
2. Manually instantiate the second IP core in the top-level file of the slave core's example design,

```
<variation_name>_example_design\simulation\
<variation_name>_example_sim.v.
```

3. Connect the master and slave by following the usual PLL sharing flow.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Minimum Pulse Width Timing Failure

Designs targeting Stratix V devices at speeds greater than 500MHz might experience minimum pulse width timing failure.

Affected Configurations

This issue affects designs targeting Stratix V devices at speeds greater than 500MHz.

Design Impact

The issue manifests as a minimum pulse width timing failure.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Write Timing Violation at 550MHz

Designs targeting Stratix V devices at 550MHz may produce write timing violations.

Affected Configurations

This issue affects designs targeting Stratix V devices at 550MHz.

Design Impact

The failure appears as negative slack values for both setup and hold, in the range of -10ps to -50ps.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation Fails with “Undefined System Task Call” Error

An issue with the JTAG Avalon master can cause simulation to fail with the following error message:

```
Error-[UST] Undefined System Task Call  
submodules/altera_pli_streaming.v, 53  
Undefined System Task call to '$do_transaction'.
```

Affected configurations

This issue affects all UniPHY-based external memory interfaces that use the internally instantiated JTAG Avalon master for the CSR port or the Efficiency Monitor and Protocol Checker.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to remove the `altera_pli_streaming` file from the list of files used in the simulation if the programming language interface (PLI) is turned off.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Unable to Directly Recompile 10.1 Design in 11.0

A design compiled in the Quartus II software version 10.1 cannot be directly recompiled in version 11.0, for speeds greater than 500 MHz.

Affected configurations

This issue affects designs targeting Stratix V devices at speeds greater than 500 MHz.

Design Impact

The 10.1 design cannot be directly recompiled in 11.0.

Workaround

The workaround for this issue is to load the `<variation_name>.v` file generated by the version 10.1 MegaWizard Plug-In Manager into the version 11.0 MegaWizard Plug-In Manager and regenerate the IP core in version 11.0.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Using UniPHY-based Memory IP with SOPC Builder

A workaround is necessary to enable UniPHY-based memory IP support with SOPC Builder.

Affected Configurations

This issue affects all UniPHY-based designs with SOPC Builder.

Design Impact

The workaround is necessary or else the design fails.

Workaround

Perform the following steps to enable UniPHY-based memory IP support in SOPC Builder:

1. On the **Controller Settings** tab in the QDR II and QDR II+ SRAM Controller with UniPHY parameter editor, turn on **Generate power-of-2 data bus widths for SOPC Builder**.
2. On the **Controller Settings** tab in the QDR II and QDR II+ SRAM Controller with UniPHY parameter editor, turn on **Generate SOPC Builder compatible resets**.
3. After generating your external memory interface IP system, open your **.sopc** file in a text editor. In the **.sopc** file, locate lines similar to the following (where *<instance_name>* is the instance name of your IP core):

```
//reset sources mux, which is an e_mux
assign reset_n_sources = ~(~reset_n |
0 |
0 |
~<instance_name>_avl_resetrequest_n_from_sa |
~<instance_name>_avl_resetrequest_n_from_sa);
```

Replace each occurrence of *~<instance_name>_avl_resetrequest_n_from_sa* with 0 (zero), so that the above snippet becomes as follows:

```
//reset sources mux, which is an e_mux
assign reset_n_sources = ~(~reset_n |
0 |
0 |
0 |
0);
```

4. Manually reconnect the UniPHY reset inputs (*global_reset_n* and *soft_reset_n*) in the SOPC Builder-generated top-level file (*system.v*), as follows:

```
.global_reset_n (reset_n_sources),
.soft_reset_n (reset_n_sources),
```

Solution Status

This issue will not be fixed.

Using Avalon-MM Traffic Generator and BIST Engine

A workaround is necessary to enable the Avalon-MM Traffic Generator and BIST Engine.

Affected Configurations

This issue affects all UniPHY-based configurations using the Avalon-MM Traffic Generator and BIST Engine.

Design Impact

The workaround is necessary or else the Avalon-MM Traffic Generator and BIST Engine fails.

Workaround

Perform the following steps to enable the workaround:

1. On the **Controller Settings** tab in the QDR II and QDR II+ SRAM Controller with UniPHY parameter editor, turn on **Generate power-of-2 data bus widths for SOPC Builder**.
2. On the **Controller Settings** tab in the QDR II and QDR II+ SRAM Controller with UniPHY parameter editor, turn on **Generate SOPC Builder compatible results**.
3. Manually reconnect the reset input (reset_n) in the top-level file (system.v), as follows:

```
.reset_n (reset_n_sources),
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation Fails when Generating VHDL for Designs Using Nios II-based Sequencer

For designs using the Nios II-based sequencer, simulation can fail when generating VHDL output.

Affected configurations

This issue affects designs using the Nios II-based sequencer and VHDL.

Design Impact

Simulation fails.

Workaround

The workaround for this issue requires that you manually modify certain files.

1. Look for three `.vhd` files with file names beginning with a string similar to the following:

`dut_dut_e0_if0_p0_qsys_sequencer_cpu_inst_jtag_debug_module` where `<dut>` is the name that you have specified for your project.

2. Open each of the three files in a text editor and add the following two lines to the beginning of each file:

```
library altera_mf;  
use altera_mf.altera_mf_components.all;
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys

The `alt_mem_if` interface supports the sharing of PLLs, DLLs, and OCTs using a sharing conduit; however, the conduit supports only point-to-point connections in Qsys, and therefore cannot be used to share a single master with multiple slaves.

Affected configurations

This limitation affects UniPHY-based designs built using Qsys.

Design Impact

The sharing of a single master with multiple slaves is not supported.

Workaround

There is no workaround for this limitation.

Solution Status

This issue will not be fixed.

Conduit Error Messages Displayed in Qsys

When generating a UniPHY-based IP core in Qsys, warning messages may appear stating that a given signal must be connected to a conduit. You may ignore such messages.

Affected configurations

This issue affects UniPHY-based designs generated with Qsys.

Design Impact

This issue has no design impact.

Workaround

Ignore the warning messages stating that a given signal must be connected to a conduit.

Solution Status

This issue will not be fixed.

Example Design Simulation May Fail in NC Sim

The autogenerated example design can fail during simulation in NC Sim.

Affected configurations

This issue affects all configurations.

Design Impact

This issue can cause the autogenerated example design to fail during simulation in NC Sim.

Workaround

Do not attempt to simulate the autogenerated example design in NC Sim.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Example Design Can Fail For Certain Parameterizations

The autogenerated example design can fail for parameterizations with `byteenables` (data mask) disabled and burst length greater than the rate ratio.

Affected configurations

This issue affects UniPHY-based designs generated with `byteenables` (data mask) disabled and burst length greater than the rate ratio.

Design Impact

This issue causes the example design to fail.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation of Example Designs Can Fail or Produce Warnings

The example design for simulation may fail to compile or trigger compiler warnings in either the VCS or NC Sim simulators, if the simulation scripts are generated from NativeLink.

Affected Configurations

This issue affects all simulations of the generated example design.

Design Impact

Simulation in NC Sim or VCS may fail; other simulators may issue warning messages.

Workaround

The following workarounds apply to this issue:

- For simulation in VCS, add the `-debug_pp` option to the `.vcs` file generated by NativeLink.
- For simulation in NC Sim or any other simulator, remove the `$vcdpluson;` line from the `<variation_name>_example_design/simulation/<variation_name>_example_sim/submodules/status_checker.sv` file.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Compilation of a UniPHY Example Design Can Produce Warnings

If you compile a UniPHY-based example design in the Quartus II software, TimeQuest may produce warning messages similar to the following:

```
Warning: Ignored filter at altera_reset_controller.sdc (17):
*|alt_rst_sync_up1|altera_rest_synchronizer_int_chain*|aclr could not
be matched with a pin
Warning: Ignored set_false_path at altera_reset_controller.sdc (17):
Argument <from> is an empty collection
```

Affected Configurations

This issue affects all UniPHY-based example designs.

Design Impact

Warning messages are displayed.

Workaround

You may safely ignore these warning messages. To prevent these warning messages from appearing, you can modify the Qsys-generated Synopsys Design Constraints file `altera_reset_controller.sdc` so that the paths mentioned in the warnings conform to the specific hierarchy of your design. (Be aware that any changes that you make to the `.sdc` file might be overwritten if you regenerate your IP core.)

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

VHDL-only Simulation Not Supported

VHDL-only simulation is not supported in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

Affected Configurations

This issue affects all designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to use a mixed Verilog-VHDL simulator.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

When you specify VHDL output for the QDR II and QDR II+ SRAM Controller with UniPHY and attempt to simulate using NativeLink, NativeLink fails and reports that it cannot find the file `<design_name>.vho` in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to not use NativeLink for simulations of VHDL designs, but to set up simulation manually instead.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.0 of the Quartus II software, when a user specifies VHDL output for the QDR II and QDR II+ SRAM Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file `<design_name>.vho` in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to edit the `<design_name>.vhd` file and remove the line similar to the following:

```
-- IPFS_FILES : <design_name>.vho
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Timing-related Warning Messages When Sharing PLLs on Stratix V Devices

When instantiating a design in PLL/DLL slave mode on a Stratix V device, the TimeQuest Timing Analyzer may display warning messages similar to the following:

```
Warning: Ignored filter at slave_report_timing_core.tcl(176):
slave_inst0|controller_phy_inst|memphy_top_inst|umemphy|uio_pads|
dq_ddio[1].ubidir_dq_dqs|altdq_dqs2_inst|thechain|clkin could not be
matched with a keeper or register or port or pin or cell or net

Warning: Command get_path failed
```

Affected Configurations

This issue affects Stratix V designs instantiated in PLL/DLL slave mode.

Design Impact

The resulting timing analysis is incorrect.

Workaround

This issue has no workaround. The warning messages can be safely ignored; however, do not rely on the accuracy of the resulting timing analysis.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Reset Synchronizer May Cause Design to Fail Timing

Systems generated with SOPC Builder or Qsys may fail timing closure due to paths that include a reset synchronizer.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails timing closure.

Workaround

A workaround for this issue is to apply the following constraint in the TimeQuest Timing Analyzer:

For SOPC Builder:

```
set_false_path -from {dut_sopc_top_reset_clk_0_domain_synch_module:  
dut_sopc_top_reset_clk_0_domain_synch*}
```

For Qsys:

```
set_false_path -from *:rst_controller*|*:alt_rst_sync_uql|  
altera_reset_synchronizer_int_chain[*] -to *:controller_phy_inst|  
*:memphy_top_inst|*:umemphy|*:ureset|*:ureset_*_clk|reset_reg[*]
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Compilation Fails if Synthesis Fileset is Mixed with Example Project Files

Compilation fails if the **Files** list in the **Settings** dialog box in the Quartus II software includes files from both the example project located at `<working_dir>/<variation_name>_example_design_fileset/example_project/` and the synthesis fileset located at `<working_dir>/<variation_name>`.

Affected Configurations

This issue affects all configurations.

Design Impact

Compilation fails.

Workaround

A workaround for this issue is to perform the following steps:

1. In an editor, open the `<variation_name>_driver.sv` file, located in the `<working_dir>/<variation_name>_example_design_fileset/example_project/` directory.

2. In the `<variation_name>_driver.sv` file, change the entity name `<variation_name>_reset_sync` to `<variation_name>_<num>_reset_sync`, where *num* is the same value as in the `<variation_name>_<num>_reset_sync.v` filename in the `<working_dir>/<variation_name>/` directory.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Warning Messages Displayed When Compiling for Stratix V Devices

When compiling a design for Stratix V devices, the system may display numerous PLL-related warning messages similar to the following:

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 do not have a PLL clock to compensate specified - the Fitter will attempt to compensate all PLL

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 use multiple different clock network types - the PLL will compensate for output clocks

Warning: PLL cross checking found inconsistent PLL clock settings:

Warning: Node: mem_if|controller_phy_inst|memphy_top_inst|pll1~FRACTIONAL_PLL|mcntout was found missing 1 generated clock that corresponds to a base clock with a period of: 8.000

Warning: Clock: mem_if|ddr3_pll_write_clk was found on node: mem_if|controller_phy_inst|memphy_top_inst|pll3|outclk with settings that do not match the following PLL specifications:

Warning: -multiply_by (expected: 21, found: 4264000)

Warning: -divide_by (expected: 5, found: 1000000)

Warning: -phase (expected: 0.00, found: 90.00)

These warning messages are expected and can be ignored.

Affected Configurations

This issue affects all configurations targeting Stratix V devices.

Design Impact

This issue has no design impact.

Workaround

There is no workaround for this issue. You can safely ignore the error messages.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Cannot Launch MegaWizard Plug-In Manager by Opening Example Design

You cannot reopen your project in the MegaWizard Plug-In Manager by clicking on your generated IP instantiation

`<working_dir>/<variation_name>_example_design/example_project/`

`<variation_name>_example/<variation_name>_example.v`

or

`<working_dir>/<variation_name>_example_design/simulation/<variation_name>_`

`example_sim/<variation_name>_example_sim.v`

Affected configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

To reopen your variation in the MegaWizard Plug-In Manager, follow these steps:

1. In the Quartus II software, click **MegaWizard Plug-In Manager** on the **Tools** menu.
2. Click **Edit an existing custom megafunction variation** and specify:
`<working_dir>/<variation_name>.v`.

Solution Status

This issue will not be fixed.

Example Design May Not Compile for IP Cores from Earlier Versions

The example design provided with version 10.1 may not compile with IP cores migrated from earlier versions of the Quartus II software.

Affected Configurations

This issue affects all configurations.

Design Impact

Attempting to compile the example design with IP cores migrated from earlier versions of the Quartus II software may fail with the following message:

Error:instance "ureset_driver_clk" instantiates undefined entity
"<variation_name>_reset_sync"

Workaround

The workaround for this issue is to perform the following steps:

1. In the Quartus II software, open the **Settings** dialog box on the **Assignments** menu.
2. In the **Category** tree of the **Settings** dialog box, click **Files** to display the files list.

3. Remove all the UniPHY files, including the .qip file and example project files, from the migrated project assignments.
4. Add to the project the newly generated .qip file located in the `<working_dir>/<variation_name>_example_design_fileset` directory.
5. Add to the project all of the files except for the memory model, from the directory `<working_dir>/<variation_name>_example_design_fileset/example_project`.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Calibration Failure in Earlier Versions

Designs generated in version 10.0SP1 and earlier may experience calibration failure due to unreliable asynchronous signal transfer from the AFI clock domain to the read-capture clock domain.

Affected Configurations

This issue affects full-rate IP cores generated in version 10.0SP1 and earlier of the QDR II and QDR II+ SRAM Controller with UniPHY.

Design Impact

Designs fail in calibration.

Workaround

Open the design in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY and regenerate the design.

Solution Status

This issue is fixed in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

SOPC Builder-generated Systems Cannot Serve as Top-Level Design

Systems generated with SOPC Builder cannot serve as the top-level design, because SOPC Builder automatically exports the `parallelterminationcontrol` and `seriesterminationcontrol` OCT control signals as top-level ports, but these signals must not be exposed at the top level.

Affected Configurations

This issue affects all configurations generated with SOPC Builder.

Design Impact

Compilation fails.

Workaround

Perform either of the following procedures to work around this issue:

- Create a top-level wrapper which instantiates the SOPC Builder-generated system, and does not make any connection to the `parallelterminationcontrol` or `seriesterminationcontrol` signals.

or

- Open the top-level SOPC Builder system file (for example, *system.v*), and delete the wire names from within the brackets for the `parallelterminationcontrol` and `seriesterminationcontrol` signals for all UniPHY cores. The resulting lines should appear as follows:

```
.parallelterminationcontrol ()  
.seriesterminationcontrol ()
```

The wire names that you delete from within the brackets must also be removed from all other locations in the top-level system file, including the top-level port list.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices

In Stratix V devices, the corner I/O banks are expected to have higher core-to-I/O and I/O-to-core delay and skew values than the other I/O banks, and are unsuitable for interfacing with external memory at frequencies above 667 MHz.

The characteristics of the corner I/O banks are not yet reflected in the Stratix V timing models available in version 10.1 of the Quartus II software; consequently, timing analysis will not accurately characterize the performance of the corner I/Os.

Affected Configurations

This issue affects all configurations targeting Stratix V devices at frequencies above 667 MHz.

Design Impact

This issue can adversely affect timing.

Workaround

Avoid using the outer I/O banks at the upper and lower sides of the device.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation Fails—PLL Clocks Out of Synchronization

During simulation, the PLL clocks lose synchronization.

Affected Configurations

This issue affects all designs.

Design Impact

This issue causes simulation failures.

Workaround

To work around this issue, follow these steps:

1. In text editor open the design file and remove the following line:

```
coverage exclude_file
```

In the ALTPLL MegaWizard interface, turn on **Create output files using the Advanced PLL parameters** and regenerate the PLL ().

Selecting VHDL Gives a Verilog HDL IP Core

If you select VHDL in the MegaWizard interface and generate a QDR II and QDR II+ SRAM Controller with UniPHY IP core, the generated core is in Verilog HDL.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The issue affects all VHDL designs.

Workaround

To generate a VHDL IP core follow these steps:

1. In a text editor open
`<Quartus II directory>\ip\altera\uniphy\lib\altera_uniphy_qdrii_hw.tcl.`

2. Search for the string "LANGUAGE" that appears in the following code:

```
append param_str ",LANGUAGE=[get_generation_property HDL_LANGUAGE]"
```

3. Change this line to the following code:

```
append param_str ",LANGUAGE=vhdl"
```

4. Continue searching for the next occurrence of the string "LANGUAGE" which appears in the following code:

```
if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
    add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
    puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \${::quartus(qip_path) ${outputname}.v\]"
} else {
```

```
add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\${::quartus(qip_path) ${outputname}.vhd\"]"
}
```

5. Comment out the if line, the else line, and the block of code in the conditional section so that the code in the "else" block always executes, similar to the following code:

```
# if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
#   add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
#   puts $qipfile "set_global_assignment -name VERILOG_FILE \[file join
join \${::quartus(qip_path) ${outputname}.v\"]"
# } else {
add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\${::quartus(qip_path) ${outputname}.vhd\"]"
# }
```

6. Use the MegaWizard interface to generate a UniPHY-based IP core.



To generate a Verilog HDL IP core, restore the original `altera_uniphy_qdrii_hw.tcl` file.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY IP core.

BSF File Not Generated

The IP core does not generate a BSF file, and therefore is not compatible with workflows requiring a BSF file.

Affected Configurations

This issue affects all configurations.

Design Impact

Errors are likely to occur with workflows using the Schematic Editor or Symbol Editor.

Workaround

Do not use the Schematic Editor or the Symbol Editor with the IP core.

Solution Status

This issue is fixed in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

Global Signal Assignments Not Applied

The Fitter sometimes does not honor GLOBAL signal assignments applied by the `<variation_name>_pin_assignments.tcl` script.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no impact on the correctness of the design, but can result in suboptimal resource placement and can contribute to difficulties in achieving timing closure.

Workaround

To determine whether GLOBAL assignments are properly applied, check the Fitter Report and verify whether any GLOBAL signal assignment referring to a PLL output port (for example, `...|auto_generated|clk[*]`) appears in the **Ignored Assignments** section.

If there is a GLOBAL assignment to a PLL output port listed in **Ignored Assignments**, you can correct the problem by running Analysis & Synthesis and then running the Fitter. You should then verify in the Fitter Report that the assignment is no longer ignored.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation Error

Inconsistency between module definition and instantiation may cause some simulators to produce an error message.

Affected Configurations

This issues affects designs targeting Arria II GX devices.

Design Impact

Some simulators may issue an error message reporting that a given port is unknown.

Workaround

The workaround for this issue is to manually edit the `oct_control.v` and `clock_pair_generator_config.v` files, and remove specific port names from each, as described in [Table 23-3](#) and [Table 23-4](#):

Table 23-3. Port Names to Remove from `clock_pair_generator_config.v`

File:	<code><variation_name>/rtl/<variation_name>_clock_pair_generator_config.v</code>
Module:	<code>arriaii_pseudo_diff_out</code>
Instance:	<code>pseudo_diffa_0</code>
Port names to remove:	<code>.dtc</code> <code>.dtcbar</code> <code>.oebout</code> <code>.oeout</code> <code>.dtcin</code> <code>.oein</code>

Table 23-4. Port Names to Remove from `oct_control.v`

File:	<code><variation_name>/rtl/<variation_name>_oct_control.v</code>
Module:	<code>arriaii_termination_logic</code>
Instance:	<code>sd2a_0</code>
Port names to remove:	<code>.scanout</code> <code>.s2pload</code> <code>.scanclk</code> <code>.scanenable</code> <code>.scanin</code> <code>.serdata</code>

Solution Status

This issue is fixed in version 10.0SP1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

Incorrect Clock Uncertainty

A clock uncertainty related to the read FIFO clocked by DQS can result in inaccurate setup and hold slack values.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can cause setup and hold slack values to be inaccurate.

Workaround

The workaround for this issue is to manually edit the PHY `.sdc` file located in the `<variation_name>/constraints/` directory, and add the following two lines to the Multicycle Constraints section of the file:

```
set_max_delay -from *ddio_in_inst_regout* -0.05
```

```
set_min_delay -from *ddio_in_inst_regout* [expr -$tCYC + 0.05]
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

IP Core May Not Operate Below 167MHz

The IP core may not operate reliably at memory clock frequencies less than 167MHz.

Affected Configurations

This issue affects configurations targeting Stratix III or Stratix IV devices.

Design Impact

Designs targeting memory clock frequencies less than 167MHz may not function properly.

Workaround

Do not use the IP core at memory clock frequencies less than 167MHz for Stratix III or Stratix IV devices.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

UniPHY DQS Clock Buffer Location

The DQS clock buffer location for the UniPHY can cause hold time violations when placed suboptimally. The Quartus II software may suboptimally place the DQS clock buffer on a global or dual-regional clock after reentering the FPGA, so that it can be routed to the write side of the read capture FIFO buffer.

Affected Configurations

The issue affects all configurations.

Design Impact

You may see hold time failures on the capture clocks in core logic.

Workaround

Create a location assignment on the buffer to the same edge as the memory interface (for example `EDGE_BOTTOM`).

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

IP Functional Simulation Model

The wizard-generated IP core functional simulation model (.vho) file for VHDL designs is functionally incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use an IP core functional simulation model to simulate your design.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

No Link to User Guide from Wizard

The wizard does not have a link to the *QDR II and II+ SRAM Controller with UniPHY User Guide*.

Affected Configurations

The issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Access the *QDR II and II+ SRAM Controller with UniPHY User Guide* from the Altera website.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

QDR II SRAM Emulated Mode

If you turn on **×36 emulated mode**, you must change the **CQ Width** to 2.

Affected Configurations

The issue affects all ×36 emulated designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Revision History

Table 24–1 shows the revision history for the RapidIO MegaCore function.



 For more information about the new features, refer to the *RapidIO MegaCore Function User Guide*.

Table 24–1. RapidIO MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> ■ Preliminary support for Stratix V devices ■ Support for Custom PHY IP core in variations that target a Stratix V device ■ Final support for Arria II GZ, Cyclone III LS, and Cyclone IV GX devices ■ HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices
10.1 SP1	February 2011	Maintenance release
10.1	December 2010	<ul style="list-style-type: none"> ■ Support for Qsys system integration tool ■ Read-only version of Port 0 Local AckID CSR
10.0 SP1	September 2010	Maintenance release
10.0	July 2010	<ul style="list-style-type: none"> ■ Preliminary support for Cyclone IV GX devices. ■ Support for configurable number of link-request attempts to be sent before fatal error, after timeout on link-response ■ Support for order preservation between read and write requests that come in on the Avalon-MM interface ■ Removed support for Stratix GX devices

Errata

Table 24–2 shows the issues that affect the RapidIO MegaCore function v11.0, v10.1 SP1, v10.1, v10.0 SP1, and v10.0.

 Not all issues affect all versions of the RapidIO MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.


 For Qsys and SOPC Builder errata, which might affect the RapidIO MegaCore function and other IP cores, refer to the *Quartus II Software Release Notes*.

Table 24-2. RapidIO MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		11.0	10.1 SP1	10.1	10.0 SP1	10.0
15 Jul 11	Qsys Appears to Allow Larger Revision IDs Than are Implemented	Fixed	✓	✓	—	—
1 Jul 11	Ignored set_false_path and Ignored filter Warnings for Stratix V Variations	✓	—	—	—	—
15 May 11	Cannot Simulate Qsys Testbench VHDL Model	✓	—	—	—	—
	Warning Message Indicates Preliminary Support for Cyclone IV GX Devices	✓	—	—	—	—
	Receive Buffer Can Overflow	Fixed	✓	✓	✓	✓
	User Guide Does Not Clarify that Migration from SOPC Builder to Qsys Changes Port Names	Fixed	✓	✓	—	—
	Device and Assembly Register Values Might Lose MSBs	Fixed	✓	✓	—	—
	Certain Changes Made in the RapidIO Parameter Editor are Ignored	Fixed	✓	✓	✓	✓
	Changes Made to the Reference Clock in the ALTGX Parameter Editor are Ignored	Fixed	✓	✓	✓	✓
15 Feb 11	Warning Message Indicates Preliminary Support for Arria II GX Devices	—	Fixed	✓	—	—
	Parameter Values Modified in SOPC to Qsys Conversion	—	Fixed	✓	—	—
	Generation Stalls in Arria GX and Stratix II GX Designs	—	Fixed	✓	✓	✓
15 Jan 11	Cannot Regenerate RapidIO MegaCore Function with Read-only .qip File	✓	✓	✓	✓	✓
15 Dec 10	Some MegaCore Variations Return Incorrect Read Data	—	—	Fixed	✓	✓
	Some Cyclone III Designs Fail Hold Time Requirements in TimeQuest Timing Analyzer	—	—	Fixed	✓	✓
	Migrated Designs Automatically Set to Seven link-request Attempts	—	—	—	Fixed	✓
	Stratix II GX Transceiver Transmitter Buffer Power Does Not Regenerate Correctly	—	—	—	Fixed	✓
	Unsupported Input Clock Frequencies Available in RapidIO Parameter Editor	—	—	—	Fixed	✓
15 Aug 10	RapidIO Parameter Editor Does Not Warn That Small Cyclone IV GX Devices Are Not Supported	✓	✓	✓	✓	✓
15 Jul 10	The Demonstration Testbench May Fail for Some RapidIO Variations	✓	✓	✓	✓	✓
	Incorrect cmu_pll_inclock_period in Stratix II GX and Arria GX Designs	✓	✓	✓	✓	✓
	Critical Warning Displays if System Clock and Reference Clock Have Same Source	✓	✓	✓	✓	✓
15 Nov 09	Some Variations With High Reference Clock Frequency Generate Critical Timing Warnings	✓	✓	✓	✓	✓
01 Nov 08	Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled	✓	✓	✓	✓	✓

Qsys Appears to Allow Larger Revision IDs Than are Implemented

The RapidIO MegaCore function supports device revision ID values (values in the `DEVICE_REV` field of the Device Information CAR at offset 0x04 in the capability register space) from 0 to 0xFFFFFFFF, stored in a 32-bit word. The RapidIO parameter editor that appears when you include a RapidIO MegaCore function in your Qsys design shows the Revision ID as a 64-bit parameter. If you set the Revision ID to a value greater than 0xFFFFFFFF, only the least significant 32 bits are maintained, and no warning message is generated.

Affected Configurations

All RapidIO variations generated using Qsys.

Design Impact

If the user-configured device revision ID value is greater than 0xFFFFFFFF, the actual configured Revision ID value is different.

Workaround

Ensure that you configure the device revision ID parameter only with values between 0 and 0xFFFFFFFF, inclusive. However, refer to [“Device and Assembly Register Values Might Lose MSBs” on page 24–6](#).

Solution Status

This issue is fixed in version 11.0 of the RapidIO MegaCore function.

Ignored `set_false_path` and Ignored filter Warnings for Stratix V Variations

When you compile a RapidIO MegaCore variation that targets a Stratix V device, the following warning messages appear:

```
Warning: Ignored filter: *alt_xcvr_csr_<suffix> could not be matched with a register
```

```
Warning: Ignored set_false_path: Argument <to> is an empty collection for various values of <suffix>.
```

Affected Configurations

This issue affects all RapidIO MegaCore function variations that target a Stratix V device.

Design Impact

This issue has no design impact. You can ignore these warning messages.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Cannot Simulate Qsys Testbench VHDL Model

The Qsys-generated VHDL testbench simulation model and the Qsys-generated Tcl script to run simulation with the VHDL testbench simulation model are defective.

Affected Configurations

This issue affects all RapidIO MegaCore function variations generated with a VHDL testbench simulation model in Qsys.

Design Impact

The RapidIO MegaCore function cannot simulate.

Workaround

To avoid this issue, generate and simulate with a Verilog HDL testbench simulation model.

To fix the problem manually, after you generate your Qsys system, follow these steps:

1. Change directory to
`<Qsys_sys_dir>/testbench/<Qsys_sys_dir>_tb/simulation/submodules.`
2. In a text editor, open the file
`<Qsys_sys_dir>_tb-<Qsys_sys_dir>_inst-<Rapidio_instance_name>.vho.`
3. Comment out all lines that include any of the following signal names:
 - `io_m_rd_clk`
 - `io_m_wr_clk`
 - `io_s_rd_clk`
 - `io_s_wr_clk`
 - `mmt_m_clk`
 - `mmt_s_clk`
 - `sys_mmt_s_clk`
4. Save and close the file.
5. Change directory to `<Qsys_sys_dir>/testbench.`
6. In a text editor, open the file `vsim_setup.tcl.`
7. Replace `vlog` with `vcom` in the following line:

```
vlog
"$QSYS_SIMDIR/<Qsys_sys_dir>_tb/simulation/submodules/<Qsys_sys_dir>_tb-<Qsys_sys_dir>_inst-<Rapidio_instance_name>.vho"
```

to create the following replacement line:

```
vcom
"$QSYS_SIMDIR/<Qsys_sys_dir>_tb/simulation/submodules/<Qsys_sys_dir>_tb-<Qsys_sys_dir>_inst-<Rapidio_instance_name>.vho"
```

8. Save and close the file.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Warning Message Indicates Preliminary Support for Cyclone IV GX Devices

The RapidIO MegaCore function v11.0 provides final support for Cyclone IV GX devices. However, when your RapidIO MegaCore function targets a Cyclone IV GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All RapidIO variations that target a Cyclone IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Receive Buffer Can Overflow

The Rx buffer in the Transport layer can overflow.

Affected Configurations

All RapidIO variations that instantiate a Transport layer.

Design Impact

Received packets may become corrupted in the Rx buffer.

Workaround

To avoid this issue, ensure that you do not fill the Rx buffer.

Solution Status

This issue is fixed in version 11.0 of the RapidIO MegaCore function.

User Guide Does Not Clarify that Migration from SOPC Builder to Qsys Changes Port Names

When you migrate an SOPC Builder system that contains a RapidIO MegaCore function to a Qsys system, many of the RapidIO MegaCore function signal names change. Signal names that have the `_<variation>` suffix in the SOPC Builder system, instead have the suffix `_from_the_<variation>` or `_to_the_<variation>` in the Qsys system. The suffix for each signal depends on the signal direction.

In a Qsys system, you can control the name of any exported signal. However, the issue should be documented in the *RapidIO MegaCore Function User Guide*.

The following signals are affected: arxwlevel, atxovf, atxwlevel, buf_av0, buf_av1, buf_av2, buf_av3, char_err, ef_ptr, error_capture_destination_id, error_capture_ftype, error_capture_letter, error_capture_mbox, error_capture_msgseg_or_xmbox, error_capture_source_id, error_capture_ttype, error_detect_illegal_transaction_decode, error_detect_illegal_transaction_target, error_detect_message_error_response, error_detect_message_format_error, error_detect_message_request_timeout, error_detect_packet_response_timeout, error_detect_unsolicited_response, error_detect_unsupported_transaction, gxb_powerdown, gxbpll_locked, master_enable, multicast_event_rx, multicast_event_tx, packet_accepted, packet_cancelled, packet_crc_error, packet_not_accepted, packet_retry, packet_transmitted, port_error, port_initialized, rd, reconfig_clk, reconfig_fromgxb, reconfig_togxb, rx_errdetect, rx_packet_dropped, rxclk, rxgxbclk, symbol_error, td, txclk.

Clock and reset signal renaming depends on the conduit names you provide in Qsys following the migration.

Affected Configurations

All RapidIO variations generated with the SOPC Builder flow and migrated to the Qsys system integration tool.

Design Impact

After migration of your design to the Qsys system integration tool, you must manually rename the affected signals in the RapidIO MegaCore function instantiation in the HDL code.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 11.0 of the *RapidIO MegaCore Function User Guide*.

Device and Assembly Register Values Might Lose MSBs

In RapidIO variations that are generated with Qsys and target a device other than a Cyclone IV GX device, the device and assembly register (capability registers at offsets 0x00 to 0x0C) non-zero field values whose decimal (base 10) representation has four or fewer decimal digits are truncated such that the two most significant decimal digits are zeroed. Leftmost zero digits are ignored for purposes of this count. No warning message is generated.

In the case of the device revision ID field, the two leftmost decimal digits are truncated if the decimal representation has eight or fewer decimal digits, rather than four or fewer decimal digits.

For example, if the device revision ID is 0x5F54433, the decimal representation is 99,959,859. This representation has eight digits, so the two most significant digits are truncated, resulting in the decimal value 959859.

Affected Configurations

All RapidIO variations generated using Qsys that target a device other than a Cyclone IV GX device.

Design Impact

In an affected configuration, if a device or assembly register value has four or fewer significant decimal digits (leftmost zeroes are not counted), the actual configured register value is missing the two most significant decimal digits. In the case of the device revision ID, if the value has eight or fewer significant decimal digits, the actual configured register value is missing the two most significant decimal digits. In these cases, the device and assembly register values are incorrect.

Workaround

To correct this issue in your RapidIO MegaCore function, after you generate your Qsys system and before you compile, follow these steps:

1. Open the file `<sysdir>/synthesis/submodules/altera_rapidio_<variation_string>.v` in a text editor. `<sysdir>` is the output directory path you specify in Qsys, and `<variation_string>` is an arbitrary alphanumeric string generated by Qsys to specify your RapidIO variation.
2. Correct the values of the signals that correspond to the individual register fields according to the register-field signal-name correspondence shown in [Table 24-3](#). Specify the correct hexadecimal value for each parameter.

Table 24-3. Signals that Correspond to Device and Assembly Register Fields

Register Field	Signal Name	Format of Corrected Value
Device ID	signal_wire10	16'hXXXX
Vendor ID	signal_wire11	16'hXXXX
Revision ID	signal_wire12	32'hXXXXXXXX
Assembly ID	signal_wire13	16'hXXXX
Assembly Vendor ID	signal_wire14	16'hXXXX
Assembly Revision ID	signal_wire15	16'hXXXX
Extended feature pointer	signal_wire16	16'hXXXX

Solution Status

This issue is fixed in version 11.0 of the RapidIO MegaCore function.

Certain Changes Made in the RapidIO Parameter Editor are Ignored

If you modify the data rate, reference clock frequency, or $1\times/4\times$ setting in an existing RapidIO MegaCore function using the RapidIO parameter editor, and then generate the RapidIO MegaCore function, the transceiver is generated with the previous data rate, reference clock frequency, and $1\times/4\times$ setting. The change does not propagate to the ALTGX megafunction.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target.

Design Impact

The RapidIO MegaCore function data rate, reference clock frequency, and $1\times/4\times$ setting cannot be modified using the RapidIO parameter editor.

Workaround

To change the data rate, reference clock frequency, or $1\times/4\times$ setting of an existing RapidIO MegaCore function, remove the existing RapidIO MegaCore function from your design, including deletion of its `<variation>_riophy_gxb.v` file, and then create a new RapidIO MegaCore function to replace it.

Solution Status

This issue is fixed in version 11.0 of the RapidIO MegaCore function.

Changes Made to the Reference Clock in the ALTGX Parameter Editor are Ignored

If you modify the reference clock frequency using the ALTGX parameter editor, and then generate the RapidIO MegaCore function, the RapidIO MegaCore function is generated with the previous reference clock frequency.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target, except variations that target a Stratix GX device.

Design Impact

The RapidIO MegaCore function reference clock frequency cannot be set using the ALTGX parameter editor.

Workaround

To avoid this issue in the RapidIO MegaCore function v9.1, set the reference clock frequency in the RapidIO parameter editor. In the RapidIO MegaCore function v9.1 SP1, that solution is not available, and you must create a new RapidIO MegaCore function instead.

Solution Status

This issue is fixed in version 11.0 of the RapidIO MegaCore function. The user can no longer edit the RapidIO transceiver reference clock frequency in the ALTGX parameter editor.

Warning Message Indicates Preliminary Support for Arria II GX Devices

The RapidIO MegaCore function v10.1 provides final support for Arria II GX devices. However, when your RapidIO MegaCore function targets an Arria II GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All RapidIO variations that target an Arria II GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 SP1 of the RapidIO MegaCore function.

Parameter Values Modified in SOPC to Qsys Conversion

If you open an SOPC Builder system in Qsys to convert it to a Qsys system, every RapidIO MegaCore function instance in the system reverts to the default disabled value for the following parameters:

- Port Write Tx Enable
- Port Write Rx Enable
- I/O read and write order preservation
- Prevent doorbell messages from passing write transactions
- Data Messages Source Operation
- Data Messages Destination Operation

Affected Configurations

All RapidIO variations in a Qsys system created by converting an SOPC Builder system to Qsys, in which one or more of the preceding parameters is enabled.

Design Impact

A design based on a Qsys system created by conversion from an SOPC Builder system might not function correctly. It might have incorrect parameter values for these RapidIO MegaCore function parameters.

Workaround

To fix the problem in your system, after conversion, edit each RapidIO MegaCore function instance in your Qsys system, and set the parameters to the correct values.

Solution Status

This issue is fixed in version 10.1 SP1 of the RapidIO MegaCore function.

Generation Stalls in Arria GX and Stratix II GX Designs

When you attempt to generate a new RapidIO MegaCore function, or regenerate an existing RapidIO MegaCore function, generation stalls. A message indicates the MegaWizard is preparing to generate the MegaCore function. The issue is due to multiple running processes to generate transceiver IP cores.

Affected Configurations

RapidIO variations that target an Arria GX or Stratix II GX device.

Design Impact

These RapidIO variations do not generate or regenerate successfully.

Workaround

To avoid this issue, kill all your running `mega_altgxbq` processes, or reboot your computer.

Solution Status

This issue is fixed in version 10.1 SP1 of the RapidIO MegaCore function.

Cannot Regenerate RapidIO MegaCore Function with Read-only .qip File

If you try to edit or regenerate a RapidIO MegaCore function whose previously generated `.qip` file has permissions set to read-only, the MegaWizard Plug-in Manager hangs when trying to generate the new version of the MegaCore function.

Affected Configurations

This issue affects all RapidIO variations.

Design Impact

Under these circumstances, you cannot edit an existing RapidIO MegaCore function.

Workaround

To avoid this issue, modify the permissions for the RapidIO MegaCore function `.qip` file to ensure it is writable before editing the RapidIO MegaCore function.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Some MegaCore Variations Return Incorrect Read Data

When a 4× RapidIO MegaCore function at data rate 5.00 Gbaud with an 8-bit device ID responds to an Avalon-MM read request, it sets the value of `io_s_rd_readdata[63:48]` incorrectly.

Affected Configurations

All 4× RapidIO variations at data rate 5.00 Gbaud with an 8-bit device ID that implement an Input/Output Avalon-MM slave Logical layer module.

Design Impact

The two most significant bytes in each 8-byte read response datum from an affected RapidIO MegaCore function variation are not reliable.

Workaround

This issue has no known workaround.

Solution Status

This issue is fixed in version 10.1 of the RapidIO MegaCore function.

Some Cyclone III Designs Fail Hold Time Requirements in TimeQuest Timing Analyzer

RapidIO ×1 variations at data rate 3.125 Gbaud that target a Cyclone III device compile with a critical warning from the TimeQuest timing analyzer indicating that timing requirements are not met and worst-case hold slack is negative.

Affected Configurations

All RapidIO ×1 variations at data rate 3.125 Gbaud that target a Cyclone III device.

Design Impact

Because these variations do not meet timing requirements using the default place and route settings, a design that contains one of these variations does not operate properly.

Workaround

Turn on the fitter setting **Perform Clocking Topology Analysis During Routing** before compiling your RapidIO design.

Solution Status

This issue is fixed in version 10.1 of the RapidIO MegaCore function.

Migrated Designs Automatically Set to Seven link-request Attempts

The RapidIO MegaCore function provided with the Quartus II software release 9.1 SP2 and earlier declares a fatal error as soon as it detects a link-request to link-response timeout. The RapidIO MegaCore function provided starting with the Quartus II software release 10.0 allows you to specify the number of times such a timeout can be detected—and a subsequent link-request reset-device control symbol be sent—before declaring a fatal error. When an earlier RapidIO MegaCore function is migrated to version 10.0, the number of times the MegaCore function sends a link-request reset-device control symbol after detecting a timeout, before declaring a fatal error, should remain at its original default value of one, for backward compatibility. However, this number in migrated MegaCore functions erroneously defaults to seven.

Seven is the default number for a new RapidIO MegaCore function version 10.0, but should not be the number to which a migrated MegaCore function defaults.

Affected Configurations

All RapidIO variations in designs migrated from a previous release of the Quartus II software.

Design Impact

By default, migrated RapidIO MegaCore functions attempt to send the link-request reset-device control symbol as many as seven times following a link-request timeout. This setting can extend the duration of the error recovery process significantly.

Workaround

After you migrate your design, to change the number of link-request attempts to the expected value of one, open the RapidIO MegaCore function parameter editor and set the **Link-request attempts** parameter to 1.

Solution Status

This issue is fixed in version 10.0 SP1 of the RapidIO MegaCore function.

Stratix II GX Transceiver Transmitter Buffer Power Does Not Regenerate Correctly

When you regenerate an existing RapidIO MegaCore function that use the high-speed transceivers on a Stratix II GX device, the transmitter buffer power (VCCH) reverts to the default value 1.2 V. The compiler complains about an invalid combination of I/O standard, common mode voltage, analog power voltage, and data rate.

Affected Configurations

All RapidIO variations that use the high-speed transceivers on a Stratix II GX device.

Design Impact

A design that contains one of these variations cannot compile successfully.

Workaround

To avoid this issue, perform the following workaround to regenerate the high-speed transceiver with the correct VCCH value:

1. In the Quartus II software, on the Tools menu, click **MegaWizard Plug-In Manager**.
2. In the MegaWizard Plug-In Manager, turn on **Edit an existing custom megafunction variation**.
3. Click **Next**.
4. In the File name field, select the file `<RapidIO_instance_name>.v`.
5. Click **Next**.
6. On the **Physical Layer** page, click **Configure Transceiver**.
7. In the transceiver parameter editor, on the **Tx Analog** page, for **What is the transmitter buffer power (VCCH)?**, select the correct voltage.
8. Click **Finish**.
9. To regenerate the RapidIO MegaCore function high-speed transceiver with the issue resolved, click **Finish**.

You can now compile your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue is fixed in version 10.0 SP1 of the RapidIO MegaCore function.

Unsupported Input Clock Frequencies Available in RapidIO Parameter Editor

The RapidIO parameter editor offers the following unsupported input clock frequencies for RapidIO MegaCore functions that target a Cyclone IV GX device:

- 78.125 MHz at data rate 1.250 Gbaud
- 78.125 MHz and 500 MHz at data rate 2.500 Gbaud
- 78.125 MHz, 97.65625 MHz, 195.3125 MHz, and 390.625 MHz at data rate 3.125 Gbaud

If you select one of these input clock frequencies, the closest supported input clock frequency is implemented in the RapidIO MegaCore function variation.

Affected Configurations

All RapidIO variations that target a Cyclone IV GX device.

Design Impact

The transceiver block in the RapidIO variation is configured with a different input clock frequency than the frequency you specified.

Workaround

Avoid selecting an unsupported input clock frequency in the RapidIO parameter editor.

Solution Status

This issue is fixed in version 10.0 SP1 of the RapidIO MegaCore function.

RapidIO Parameter Editor Does Not Warn That Small Cyclone IV GX Devices Are Not Supported

The RapidIO MegaCore function device support for Cyclone IV GX devices includes only the EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices. This restriction is not explained in the *RapidIO MegaCore Function User Guide*. In addition, the RapidIO parameter editor does not enforce this restriction: if you specify another Cyclone IV GX device or allow the Quartus II software to automatically determine the device, RapidIO MegaCore function generation proceeds with no warning, but compilation fails.

Affected Configurations

RapidIO variations that target a Cyclone IV GX device, if the specific device is automatically determined by the Quartus II software, or is an EP4CGX15, EP4CGX22, or EP4CGX30 device.

Design Impact

These RapidIO variations do not compile successfully.

Workaround

To avoid this issue, target your Cyclone IV GX RapidIO MegaCore function to an EP4CGX50, EP4CGX75, EP4CGX110, or EP4CGX150 device.

Solution Status

The restriction is clarified in version 10.1 of the *RapidIO MegaCore Function User Guide*.

The Demonstration Testbench May Fail for Some RapidIO Variations

RapidIO variations that implement an Input/Output Avalon-MM master or slave Logical layer module and target a Stratix IV GX or Arria II GX device fail simulation with an error message indicating that a signal did not have expected value. The problem is due to an uninitialized RTL parameter in the IP functional simulation model.

Affected Configurations

RapidIO variations that implement an Input/Output Avalon-MM master or slave Logical layer module and target an Arria II GX or Stratix IV GX device.

Design Impact

These RapidIO variations cannot simulate successfully with the demonstration testbench.

Workaround

To avoid this issue, regenerate your IP functional simulation model with the `quartus_map` command-line option `SIMGEN_RAND_POWERUP_FFS=OFF`.

The following script provides this command for the DUT and the sister RIO in the testbench, for the case of a RapidIO MegaCore function variation that instantiates all modules. To use it to regenerate your IP functional simulation model, update the file names for your variation, modify the commands with the correct device and HDL, and remove the lines that reference modules your variation does not include.

Run the script, or enter the corresponding commands, in the directory that contains all the source files.

```
#!/bin/sh

#Modify the following lines with the correct device and HDL information.
#Parameter CBX_HDL_LANGUAGE=Verilog or VHDL
#Parameter --family is one of {stratixiv, arria10gx, cycloneiv, arriagx,
stratixiigx}.

#Regenerate the IP functional simulation model for the DUT:
quartus_map --simgen \
    --simgen_parameter="CBX_HDL_LANGUAGE=Verilog,SIMGEN_RAND_POWERUP_FFS=OFF" \
    --family=stratixiv \
    --source="./rio_rio.v" \
    --source="./rio_riophy_gxb.v" \
    --source="./rio_phy_mnt.v" \
    --source="./rio_riophy_xcvr.v" \
    --source="./rio_riophy_dcore.v" \
    --source="./rio_riophy_reset.v" \
    --source="./rio_concentrator.v" \
    --source="./rio_drbell.v" \
    --source="./rio_io_master.v" \
    --source="./rio_io_slave.v" \
    --source="./rio_maintenance.v" \
    --source="./rio_reg_mnt.v" \
    --source="./rio_transport.v" \
rio.v

# Continued on next page

#Regenerate the IP Functional Simulation Model for SISTER
cp rio_rio_sister.v rio_sister_rio.v
cp rio_riophy_gxb_sister.v rio_sister_riophy_gxb.v
quartus_map --simgen \
    --simgen_parameter="CBX_HDL_LANGUAGE=Verilog,SIMGEN_RAND_POWERUP_FFS=OFF" \
    --family=stratixiv \
    --source="./rio_sister_rio.v" \
    --source="./rio_sister_riophy_gxb.v" \
    --source="./rio_phy_mnt_sister.v" \
    --source="./rio_riophy_xcvr_sister.v" \
    --source="./rio_riophy_dcore_sister.v" \
    --source="./rio_riophy_reset_sister.v" \
    --source="./rio_concentrator_sister.v" \
    --source="./rio_drbell_sister.v" \
    --source="./rio_io_master_sister.v" \
```

```
--source="./rio_io_slave_sister.v" \
--source="./rio_maintenance_sister.v" \
--source="./rio_reg_mnt_sister.v" \
--source="./rio_transport_sister.v" \
rio_sister_rio.v
```

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Incorrect cmu_pll_inclock_period in Stratix II GX and Arria GX Designs

For RapidIO variations that use the high-speed transceivers on a Stratix II GX or Arria GX device, the transceiver `cmu_pll_inclock_period` value is set incorrectly.

Affected Configurations

RapidIO variations that use the high-speed transceivers on a Stratix II GX or Arria GX device.

Design Impact

Simulation and compilation fail for the affected configurations.

Workaround

In the file `<RapidIO instance name>_riophy_gxb.v`, in the assignment to the `alt2gxb_component.cmu_pll_inclock_period` signal, assign the value $10^6 / \text{<pll_inclock frequency>}$ in place of the incorrect value.

To propagate the change to the IP functional simulation model, regenerate the model with the `quartus_map` command. Refer to the workaround for the erratum [“The Demonstration Testbench May Fail for Some RapidIO Variations”](#) on page 24-14 for the appropriate command-line options.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Critical Warning Displays if System Clock and Reference Clock Have Same Source

If the system clock and the reference clock for your RapidIO MegaCore function are driven by the same source, the Quartus II software issues a critical warning.

Affected Configurations

All RapidIO variations in designs in which the RapidIO system clock and reference clock are driven by the same source.

Design Impact

This issue has no design impact. The critical warning can be ignored.

Workaround

You can avoid the critical warning by cutting some of the nodes in the Synopsys Design Constraints File (.sdc). To obtain an .sdc compatible list of the nodes to be cut, refer to Altera solution rd07132010_207 at www.altera.com/support/kdb/solutions/rd07132010_207.html.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Some Variations With High Reference Clock Frequency Generate Critical Timing Warnings

RapidIO MegaCore function variations with reference clock frequency higher than 260 MHz that target an Arria II GX or Stratix IV GX device cause the TimeQuest timing analyzer to issue the following critical warning:

Critical Warning: Found minimum pulse width or period violations. See Report Minimum Pulse Width for details.

The warning occurs because the reference clock input pin is set to the 2.5 V I/O pin standard by default, and this I/O pin standard requires a minimum pulse width of 3.826 us, which corresponds to 260 MHz.

Affected Configurations

All RapidIO variations with reference clock frequency higher than 260 MHz that target an Arria II GX or Stratix IV GX device.

Design Impact

Designs that contain any of these RapidIO variations cannot compile with the default I/O standard assignments.

Workaround

To avoid this issue, in the Assignment Editor, assign the reference clock pin to the LVDS I/O standard.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled

Simulation of a RapidIO MegaCore function targeted to a Stratix IV device using ModelSim 6.3g with compiler optimizations enabled, may fail. Compiler optimizations are enabled by default in this version of ModelSim.

Affected Configurations

All RapidIO variations that target a Stratix IV device.

Design Impact

The IP functional simulation model of an affected configuration may produce data errors if simulated using ModelSim 6.3g.

Workaround

To avoid this issue, perform one of the following workarounds:

- Disable the ModelSim compiler optimizations by adding the `-novopt` switch to the `vsim` command, in the `<variant>_run_modelsim.tcl` script or when you call `vsim` from the command line.
- Use ModelSim 6.4a or later.

Solution Status

The issue is fixed in ModelSim 6.4a.

Revision History

Table 25–1 shows the revision history for the Reed-Solomon Compiler.



For more information about the new features, refer to the *Reed-Solomon Compiler User Guide*.

Table 25–1. Reed-Solomon Compiler Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.

Errata

Table 25–2 shows the issues that affect the Reed-Solomon Compiler v11.0, v10.1, and v10.0.



Not all issues affect all versions of the Reed-Solomon Compiler.

Table 25–2. Reed-Solomon Compiler Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices	✓	—	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—
01 Nov 08	Verilog HDL Simulation Fails	✓	✓	✓
	RS Decoder Fails When Number of Check Symbols and Symbols are Similar	✓	✓	✓

Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices

The Reed-Solomon Compiler v11.0 provides final support for Arria II GZ and Cyclone IV GX devices. However, when your Reed-Solomon Compiler targets an Arria II GZ device or a Cyclone IV GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All Reed-Solomon Compiler variations that target an Arria II GZ device or a Cyclone IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon Compiler.

Compilation Targeting a Stratix V Device Fails

Designs that include a Reed-Solomon Compiler and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

Reed-Solomon Compiler designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Verilog HDL Simulation Fails

Running a simulation with the Verilog HDL testbench results in an empty `summary_output.txt` file.

Affected Configurations

This issue affects all Verilog HDL configurations.

Design Impact

You cannot use the `summary_output.txt` file to evaluate the functionality of the design. But you can evaluate the functionality by looking at the simulation waveform.

Workaround

Run the simulation with a VHDL design and use the VHDL testbench.

Solution Status

This issue will be fixed in a future release of the Reed-Solomon Compiler.

RS Decoder Fails When Number of Check Symbols and Symbols are Similar

With the variable decoder, when the **Number of check symbols** and **Symbols per codeword** values are similar, for example, 5 and 6, respectively, the Avalon-ST interface on the source side fails and the `sop` and `eop` overlap.

Affected Configurations

This issue affects all Verilog HDL variable decoder designs.

Design Impact

The design fails simulation.

Workaround

To avoid this issue, create a VHDL design model and use the VHDL testbench.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon Compiler.

Revision History

Table 26–1 shows the revision history for Reed-Solomon II.



For information about the new features, refer to the *Reed-Solomon II MegaCore Function User Guide*.

Table 26–1. Reed-Solomon II Revision History

Version	Date	Description
11.0	May 2011	Added new status ports and timing diagrams.
10.1	December 2010	First release.

Errata

Table 26–2 shows the issues that affect the Reed-Solomon II v11.0 and v10.1.



Not all issues affect all versions of the Reed-Solomon II.

Table 26–2. Reed-Solomon II Errata

Added or Updated	Issue	Affected Version	
		11.0	10.1
15 Dec 10	Backpressure Feature is Not Supported	✓	✓
	Unsupported Variants	✓	✓
	Unable to Support Invalid Avalon-ST Packets	✓	✓

Backpressure Feature is Not Supported

Backpressure feature is not supported for 11.0 and 10.1 software release.

Affected Configurations

This issue affects all Reed-Solomon II encoder and decoder variations.

Design Impact

The core may generate erroneous output if it is backpressured, which means when out_ready signal is toggled.

Workaround

Set the out_ready signal high.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon II MegaCore function.

Unsupported Variants

Variants other than the ones targeted for OTN (Optical Transport Network) applications are not fully supported in 10.1 software.

Affected Configurations

This issue affects all Reed-Solomon II encoder and decoder variations except for the following variants:

- N=255, CHECK=16, CHANNEL=1 IRRPOL=285
- N=255, CHECK=16, CHANNEL=2 IRRPOL=285
- N=255, CHECK=16, CHANNEL=8 IRRPOL=285

Design Impact

The core might generate erroneous output for all affected variants.

Workaround

Use non-affected configurations only.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon II MegaCore function.

Unable to Support Invalid Avalon-ST Packets

The Reed-Solomon II encoder and decoder are unable to support Avalon-ST packets (codewords) that contain invalid data.

Affected Configurations

This issue affects all Reed-Solomon II encoder and decoder variations.

Design Impact

The core might generate erroneous output if `in_valid` signal is toggled during a codeword transmission.

Workaround

To avoid this problem, use only codewords with continuous valid data.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon II MegaCore function.

Revision History

Table 27–1 shows the revision history for the RLDRAM II MegaCore function.



For more information about the new features, refer to the *RLDRAM II MegaCore Function User Guide*.

Table 27–1. RLDRAM II MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	Maintenance release.
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.

Errata

Table 27–2 shows the issues that affect the RLDRAM II MegaCore function v11.0, 10.1, and 10.0.



Not all issues affect all versions of the RLDRAM II MegaCore function.

Table 27–2. RLDRAM II MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 Nov 09	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓
	Hold Timing Violation	✓	✓	✓
01 Dec 06	NativeLink Fails with the ModelSim Simulator	✓	✓	✓
01 Nov 06	Add an RLDRAM II Controller to a Project with Other Memory Controllers	✓	✓	✓
	Simulating with the NCSim Software	✓	✓	✓
	Simulating with the VCS Simulator	✓	✓	✓
	Multiple Instances of the auk_ddr_functions.vhd File	✓	✓	✓
	Gate-Level Simulation Filenames	✓	✓	✓
	Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)	✓	✓	✓
	Editing the Custom Variation (non-DQS Mode)	✓	✓	✓

The Quartus II Design Assistant Reports Critical Warning

When you compile a design with the RLDRAM II controller, the Quartus II Design Assistant reports design the following warnings:

Critical Warning: (High) Rule R101: Combinational logic used as a reset signal should be synchronized. Found 1 node(s) related to this rule.

Warning: (Medium) Rule C104: Clock signal source should drive only clock input ports.
Found 2 nodes related to this rule.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Hold Timing Violation

Hold timing violation occurs on the DQS clock reported in fast-corner timing report.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Disable the global clock promotion on dqs_clk by adding the following assignment in the Quartus II settings file (.qsf):

```
set_instance_assignment -name GLOBAL_SIGNAL OFF -to "<variation  
name>_wrapper:<variation  
name>|<variation name>_auk_rldramii_datapath:rldramii_io|<variation  
name>_auk_rldramii_dqs_group:auk_rldramii_dqs_group_*|dqs_clk[0]"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

NativeLink Fails with the ModelSim Simulator

When using NativeLink to run VHDL gate-level simulations using the ModelSim software, the simulation fails with the following error message:

```
# ** Error: (vcom-19) Failed to access library 'altera' at "altera".
```

Affected Configurations

The issue affects VHDL gate-level simulations.

Design Impact

The design does not simulate.

Workaround

The following lines need to be added to the NativeLink-generated gate-level simulation script:

```
vlib vhdl_libs/altera
vmap altera vhdl_libs/altera
vcom -work altera <Quartus installation
directory>/libraries/vhdl/altera/altera_europa_support_lib.vhd
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Add an RLDRAM II Controller to a Project with Other Memory Controllers

If you try to generate a new RLDRAM II controller in a project that already contains a DDR, DDR2, QDR II, or RLDRAM II controller, the example design gets corrupted and the compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not compile.

Workaround

To work around this issue, follow these steps:

1. Generate the RLDRAM II controller in a new project and update the required project to instantiate the new RLDRAM II controller.
2. Copy the constraints from the new RLDRAM II project to the target project.
3. Copy the new RLDRAM II design files into the target project directory.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the NCSim Software

The RLDRAM II Controller MegaCore function does not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the `-relax` switch for all calls to the VHDL or Verilog HDL analyzer.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the VCS Simulator

The RLDRAM II Controller MegaCore function does not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

For VHDL simulations, in the `<variation name>_example_driver.vhd` file, change all when statements from:

```
when std_logic_vector'("<bit_pattern>")
```

to:

```
when "<bit_pattern>"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Multiple Instances of the auk_dds_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus II project has multiple instances of the `auk_dds_functions.vhd` file (one per MegaCore function).

Affected Configurations

This issue affects all configurations.

Design Impact

The Quartus II project fails during compilation.

Workaround

Remove the **auk_dds_functions.vhd** file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing **Add/Remove Files from Project** on the Project menu. Keep only the **auk_dds_functions.vhd** file associated with the DDR or DDR2 SDRAM controller.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause the Quartus II software to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects *<project name>.vho* or *.vo* and *<project name>_v* or *_vhd.sdo* files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory, follow these steps:

1. Rename *<filename>.vho* file to *<project name>.vho*.
2. Rename *<filename>.sdo* file to *<project name>_vhd.sdo*.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory, follow these steps:

1. Rename the *<filename>.vo* file to *<project name>.vo*.
2. Rename the *<filename>.sdo* file to *<project name>_v.sdo*.
3. In the *<project name>.vo* file, change the following line to point to the *<project name>_v.sdo* file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)

Gate-level simulations may not work as expected on HardCopy II devices, because HardCopy II timing is preliminary in the Quartus II software.

Affected Configurations

This issue affects all configurations on HardCopy II devices.

Design Impact

This issue has no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Editing the Custom Variation (non-DQS Mode)

When you generate a non-DQS mode custom variation with large databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

- IP Toolbench does not reload
- IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
- IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups

Affected Configurations

This issue affects non-DQS mode designs only.

Design Impact

This issue has no design impact if you implement the workaround.

Workaround

Use one of the following workarounds:

- If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters
- If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
- If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Revision History

Table 28–1 shows the revision history for the RLDRAM II Controller with UniPHY.



For more information about the new features, refer to the *RLDRAM II Controller with UniPHY User Guide*.

Table 28–1. RLDRAM II Controller with UniPHY Revision History

Date	Version	Description
July 2011	11.0 SP1	Maintenance release
May 2011	11.0	<ul style="list-style-type: none"> Added Nios II-based sequencer Upgraded f_{MAX} (with Nios II sequencer): <ul style="list-style-type: none"> To 533 MHz for Stratix III, Stratix IV, and Stratix V devices To 400 MHz for HardCopy IV devices
December 2010	10.1	<ul style="list-style-type: none"> Added preliminary support for Arria II GZ and Stratix V Added new generated directory structure Added new OCT Sharing Interface feature Added External Memory Interface Toolkit
July 2010	10.0	<ul style="list-style-type: none"> Added width expansion feature Added error detection parity feature Added user-controlled refresh feature Added variable latency feature

Errata

Table 28–2 shows the issues that affect the RLDRAM II Controller with UniPHY v11.0, 10.1, and 10.0.



Not all issues affect all versions of the RLDRAM II Controller with UniPHY.

Table 28–2. RLDRAM II Controller with UniPHY Errata (Part 1 of 3)

Added or Updated	Issue	Affected Versions			
		11.0 SP1	11.0	10.1	10.0
15 Jul 11	Simulation fails in Riviera-PRO	✓	—	—	—
	Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations	✓	—	—	—
	Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error	✓	—	—	—

Table 28-2. RLDRAM II Controller with UniPHY Errata (Part 2 of 3)

Added or Updated	Issue	Affected Versions			
		11.0 SP1	11.0	10.1	10.0
1 Jul 11	VHDL-Generated Fileset Can Encounter Synthesis Problems	✓	✓	—	—
	UniPHY CSR Ports Not Functioning Correctly	Fixed	✓	—	—
	Stratix V Memory Interfaces May Exhibit Write Timing Failure	✓	✓	—	—
	UniPHY IP Generation Fails if Quartus II Path Contains a Space	✓	✓	—	—
	Efficiency Monitor Latency Values Are Incorrect	✓	✓	—	—
	Enable Avalon-MM Byte-Enable Signal Option Not Functional	✓	✓	—	—
	Example Project Fails to Simulate When HardCopy Compatibility Enabled	✓	✓	—	—
	NativeLink RTL Simulation May Fail	Fixed	✓	—	—
	Error Messages in ModelSim Flow for Eclipse	✓	✓	—	—
	ModelSim Waveform Viewer Shows Only clk and reset Signals	Fixed	✓	—	—
	PLL Master Required for Simulation of PLL Slave	✓	✓	—	—
	Minimum Pulse Width Timing Failure	Fixed	✓	—	—
	Efficiency Monitor Statistics Incorrect for Initial Sample	✓	✓	—	—
	Simulation Fails with “Undefined System Task Call” Error	✓	✓	—	—
	Unable to Directly Recompile 10.1 Design in 11.0	✓	✓	—	—
	Using UniPHY-based Memory IP with SOPC Builder	✓	✓	—	—
	Using Avalon-MM Traffic Generator and BIST Engine	✓	✓	—	—
	Simulation Fails when Generating VHDL for Designs Using Nios II-based Sequencer	✓	✓	—	—
	Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys	✓	✓	—	—
	Conduit Error Messages Displayed in Qsys	✓	✓	—	—
	Example Design Simulation May Fail in NC Sim	✓	✓	—	—
	Must Enable Support for Nios II ModelSim Flow in GUI	✓	✓	—	—
	Simulation of Example Designs Can Fail or Produce Warnings	✓	✓	—	—
	Compilation of a UniPHY Example Design Can Produce Warnings	✓	✓	—	—
15 Mar 11	VHDL-only Simulation Not Supported	—	Fixed	✓	—
15 Dec 10	NativeLink Simulation fails for VHDL Output	✓	✓	✓	—
	NativeLink Simulation fails for VHDL Output	—	—	—	✓
	Timing-related Warning Messages When Sharing PLLs on Stratix V Devices	✓	✓	✓	—
	Reset Synchronizer May Cause Design to Fail Timing	✓	✓	✓	—
	Compilation Fails if Synthesis Fileset is Mixed with Example Project Files	—	Fixed	✓	—
	Warning Messages Displayed When Compiling for Stratix V Devices	✓	✓	✓	—
	Cannot Launch MegaWizard Plug-In Manager by Opening Example Design	✓	✓	✓	—
	Example Design May Not Compile for IP Cores from Earlier Versions	—	Fixed	✓	—
	Calibration Failure in Earlier Versions	—	Fixed	✓	—
	SOPC Builder-generated Systems Cannot Serve as Top-Level Design	—	Fixed	✓	—
	Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices	✓	✓	✓	—

Table 28–2. RLDram II Controller with UniPHY Errata (Part 3 of 3)

Added or Updated	Issue	Affected Versions			
		11.0 SP1	11.0	10.1	10.0
15 Sept 10	Simulation Fails—PLL Clocks Out of Synchronization	✓	✓	✓	✓
15 Aug 10	Selecting VHDL Gives a Verilog HDL IP Core	✓	✓	✓	✓
	Incorrect Clock Uncertainty	—	Fixed	✓	✓
15 Jul 10	BSF File Not Generated	—	—	Fixed	✓
	Global Signal Assignments Not Applied	✓	✓	✓	✓
15 Nov 09	UniPHY DQS Clock Buffer Location	✓	✓	✓	✓
	IP Functional Simulation Model	—	—	Fixed	✓
	No Link to User Guide from Wizard	✓	✓	✓	✓
	–18 Presets Give Errors	—	Fixed	✓	✓

Simulation fails in Riviera-PRO

Simulation in Riviera-PRO may fail, with an error message suggesting that MEM_WRITE_DQS_WIDTH must contain a positive value.

Affected configurations

This issue affects all configurations.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to open the alt_mem_if_rldramii_mem_model.sv file in a text editor, and make the following changes:

1. Near the top of the file, change the parameter declaration for MEM_WRITE_DQS_WIDTH from:

```
parameter MEM_WRITE_DQS_WIDTH = "";
```

to

```
parameter MEM_WRITE_DQS_WIDTH = 1;
```

2. Further down in the file, change:

```
time [MEM_WRITE_DQS_WIDTH - 1:0] mem_dk_time;
```

to

```
time mem_dk_time[MEM_WRITE_DQS_WIDTH]
```

Solution Status

This issue will be fixed in a future version of the RLDram II Controller with UniPHY.

Erroneous Timing Failures in Designs Containing Both UniPHY and ALTMEMPHY Instantiations

Designs containing both UniPHY and ALTMEMPHY instantiations may encounter erroneous clock failures during timing analysis.

Affected configurations

This issue affects all configurations containing both UniPHY and ALTMEMPHY instantiations.

Design Impact

Timing analysis may incorrectly report that some paths are failing timing.

Workaround

The workaround for this issue is to open the UniPHY `<core_name>_report_timing.tcl` and `<core_name>_pin_map.tcl` files in an editor, and make the following change in each file:

Locate the `traverse_to_ddio_out_pll_clock` function name, and append the numeral 2 to the function name, making it `traverse_to_ddio_out_pll_clock2`.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Simulation with NC Sim or Riviera-PRO Fails with an Elaboration Error

Simulation with NC Sim or Riviera-PRO may fail with the error message: Unsupported memory slice specification using part select or indexed part select.

Affected configurations

This issue affects all configurations using the Nios II-based sequencer.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to open the `sequencer_scc_mgr.sv` file in an editor, and locate the following code:

```
integer unsigned setting_offsets[1:9];
t_setting_mask setting_masks [1:9];

generate
    if (FAMILY == "STRATIXV")
    begin
        assign setting_offsets[1:9] = '{ 'd0, 'd12, 'd17, 'd25, 'd30, 'd36, 'd0,
        'd6, 'd12 };
```



```

        assign setting_masks [1:9] = '{ 'b011111111111, 'b011111,
'b011111111, 'b011111, 'b0111111, 'b0111111, 'b0111111, 'b0111111,
'b011111111111 }';
    end
    else
    begin
        assign setting_offsets[1:9] = '{ 'd0, 'd4, 'd8, 'd12, 'd17,
'd21, 'd0, 'd4, 'd7 }';
        assign setting_masks [1:9] = '{ 'b01111, 'b01111, 'b01111,
'b11111, 'b01111, 'b00111, 'b01111, 'b00111, 'b01111 }';
    end
endgenerate

```

For Stratix V devices, replace the preceding code with the following:

```

integer setting_offsets[1:9] = '{ 'd0, 'd12, 'd16, 'd24, 'd27, 'd33, 'd0,
'd6, 'd12 }';
t_setting_mask setting_masks [1:9] = '{ 'b011111111111, 'b01111,
'b011111111, 'b0111, 'b0111111, 'b0111111, 'b0111111, 'b0111111,
'b011111111111 }';

```

For non-Stratix V device families, replace the code with the following:

```

integer setting_offsets[1:9] = '{ 'd0, 'd4, 'd8, 'd12, 'd17, 'd21, 'd0,
'd4, 'd7 }';
t_setting_mask setting_masks [1:9] = '{ 'b01111, 'b01111, 'b01111, 'b11111,
'b01111, 'b00111, 'b01111, 'b00111, 'b01111 }';

```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

VHDL-Generated Fileset Can Encounter Synthesis Problems

An error in the VHDL-generated wrapper for the synthesis fileset can result in a variety of synthesis problems.

Affected configurations

This issue affects all configurations using VHDL.

Design Impact

Synthesis problems can result.

Workaround

The workaround for this issue is to open the generated wrapper file in a text editor, and replace all ports of the form `std_logic_vector(0 downto 0)` with `std_logic`.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

UniPHY CSR Ports Not Functioning Correctly

The CSR ports in UniPHY-based interfaces do not function correctly.

Affected configurations

This issue affects all configurations using CSR ports.

Design Impact

The CSR ports do not function correctly.

Workaround

There is no workaround for this issue. Consider using the JTAG Avalon master interface instead.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Stratix V Memory Interfaces May Exhibit Write Timing Failure

Memory interfaces targeting Stratix V devices may exhibit write setup or write hold timing failures.

Affected configurations

This issue affects configurations targeting Stratix V devices.

Design Impact

Write setup or write hold timing failures occur.

Workaround

A workaround for interfaces running at 400MHz or slower is to enable the high-performance Nios II-based sequencer instead of the RTL-based sequencer.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

UniPHY IP Generation Fails if Quartus II Path Contains a Space

UniPHY IP generation fails if the installation path of the Quartus II software contains one or more spaces.

Affected configurations

This issue affects all configurations.

Design Impact

UniPHY IP generation fails.

Workaround

The workaround for this issue is to ensure that the Quatrus II installation path contains no spaces.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Efficiency Monitor Latency Values Are Incorrect

The Efficiency Monitor and Protocol Checker counts read latencies incorrectly for Avalon burst counts equal to 1; this causes the EMIF Toolkit to report incorrect values for minimum and maximum read latencies.

This issue occurs if you measure efficiency with the example design driver; however, if you use your own custom driver that does not issue an Avalon burst count size equal to 1, the error will not occur.

Affected configurations

This issue affects all configurations with Avalon burst count equal to 1.

Design Impact

Incorrect minimum and maximum read latencies are reported.

Workaround

The workaround for this issue is to use a custom driver that does not issue an Avalon burst count equal to 1.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Enable Avalon-MM Byte-Enable Signal Option Not Functional

The **Enable Avalon-MM byte-enable signal** option available on the **Controller Settings** tab in the parameter editor does not function.

Affected Configurations

This issue affects all designs.

Design Impact

The **Enable Avalon-MM byte-enable signal** option has no effect.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Example Project Fails to Simulate When HardCopy Compatibility Enabled

The example project for designs generated with **HardCopy Compatibility Mode** enabled can fail to simulate.

Affected configurations

This issue affects RLDRAM II UniPHY designs generated with **HardCopy Compatibility Mode** enabled.

Design Impact

The example project fails in simulation.

Workaround

The workaround for this issue is to modify two files, as follows:

1. In a text editor, open the file
`<variant_name>_example_design/simulation/<variant_name>_example_sim/submodules/<variant_name>_example_sim_<variant_name>_example_sim.v`
2. In the above file, change the line
`.INIT_FILE = ("dut_dut_e0_if0_p0_sequencer_rom.v")`
to
`.INIT_FILE =`
`("<variant_name>_example_sim_<variant_name>_example_sim_e0_if0_p0_sequencer_rom.v")`
3. In a text editor, open the file
`<variant_name>_example_design/simulation/<variant_name>_example_sim.qsf`
4. In the above file, add the following lines:
`set_global_assignment -name EDA_TEST_BENCH_FILE`
`<variant_name>_example_sim/submodules/hc_rom_reconfig_gen.sv -`
`section_id uniphy_rtl_simulation -hdl_version SystemVerilog_2005`

`and`

`set_global_assignment -name SOURCE_FILE`
`<variant_name>_example_sim/submodules/<variant_name>_example_sim_`
`<variant_name>_example_sim_e0_if0_p0_sequencer_rom.hex`

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

NativeLink RTL Simulation May Fail

NativeLink RTL simulation may fail and report warnings that a file could not be opened for reading.

Affected configurations

This issue affects all UniPHY protocols.

Design Impact

Simulation fails.

Workaround

The workaround for this issue is to edit the project's **.qsf** settings file and add to it all the **.hex** and **.mif** files residing in the directory:

```
<variant_name>_example_design/simulation/<variant_name>_example_sim/  
submodules/
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Error Messages in ModelSim Flow for Eclipse

Designs generated with the **Enable support for Nios II ModelSim flow in Eclipse** option enabled can produce error messages reporting attempts to read from uninitialized data locations.

Affected configurations

This issue affects RLDRAM II designs generated with the **Enable support for Nios II ModelSim flow in Eclipse** option enabled.

Design Impact

Error messages are displayed.

Workaround

There is no workaround for this issue; you may ignore the error messages.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

ModelSim Waveform Viewer Shows Only clk and reset Signals

ModelSim simulation of the example design for MegaWizard-generated systems displays only the clk and reset signals in the waveform viewer.

Affected configurations

This issue affects all MegaWizard-generated RLDRAM II Controller with UniPHY interfaces.

Design Impact

Only clk and reset waveforms are displayed.

Workaround

The workaround for this issue is as follows:

1. Open the existing `<variant_name>_example_design/simulation/<variant_name>_example_sim.qsf` file in a text editor and add the following line to the file:

```
set_global_assignment -name EDA_NATIVELINK_SIMULATION_SETUP_SCRIPT
my_wave.do -section_id eda_simulation
```

Where `<my_wave>.do` is a file name of your choice.

2. Create a ModelSim `<my_wave>.do` file in the `<variant_name>_example_design/simulation` directory.

Ensure that the `<my_wave>.do` file has the following content:

```
"
add wave dut/<variant_name>_example_sim_inst/*
run -all
"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

PLL Master Required for Simulation of PLL Slave

The example simulation design (generated in the `<variation_name>_example_design\simulation` folder) does not function correctly if the core is parameterized with **PLL Sharing Mode = Slave**, **DLL Sharing Mode = Slave**, or **OCT Sharing Mode = Slave**.

Affected configurations

This issue affects all protocols with UniPHY interfaces employing slave PLLs, DLLs, or OCTs.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to ensure that a master instantiation is provided to drive the slave. To do this, follow these steps (a PLL example is shown):

1. Generate a second, identically parameterized, IP core with **PLL Sharing Mode** set to **Master**.
2. Manually instantiate the second IP core in the top-level file of the slave core's example design,

```
<variation_name>_example_design\simulation\  
<variation_name>_example_sim.v.
```

3. Connect the master and slave by following the usual PLL sharing flow.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Minimum Pulse Width Timing Failure

Designs targeting Stratix V devices at speeds greater than 500MHz might experience minimum pulse width timing failure.

Affected Configurations

This issue affects designs targeting Stratix V devices at speeds greater than 500MHz.

Design Impact

The issue manifests as a minimum pulse width timing failure.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Efficiency Monitor Statistics Incorrect for Initial Sample

The initial statistics produced by the Efficiency Monitor are likely to be incorrect while the interface is calibrating.

Affected configurations

This issue affects RLDRAM II UniPHY designs.

Design Impact

The initial data produced by the Efficiency Monitor may be incorrect.

Workaround

The workaround for this issue is to wait for calibration to finish before rereading the statistics from the Efficiency Monitor.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Simulation Fails with “Undefined System Task Call” Error

An issue with the JTAG Avalon master can cause simulation to fail with the following error message:

```
Error-[UST] Undefined System Task Call  
submodules/altera_pli_streaming.v, 53  
Undefined System Task call to '$do_transaction'.
```

Affected configurations

This issue affects all UniPHY-based external memory interfaces that use the internally instantiated JTAG Avalon master for the CSR port or the Efficiency Monitor and Protocol Checker.

Design Impact

The design fails in simulation.

Workaround

The workaround for this issue is to remove the `altera_pli_streaming` file from the list of files used in the simulation if the programming language interface (PLI) is turned off.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Unable to Directly Recompile 10.1 Design in 11.0

A design compiled in the Quartus II software version 10.1 cannot be directly recompiled in version 11.0, for speeds greater than 500 MHz.

Affected configurations

This issue affects designs targeting Stratix V devices at speeds greater than 500 MHz.

Design Impact

The 10.1 design cannot be directly recompiled in 11.0.

Workaround

The workaround for this issue is to load the `<variation_name>.v` file generated by the version 10.1 MegaWizard Plug-In Manager into the version 11.0 MegaWizard Plug-In Manager and regenerate the IP core in version 11.0.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Using UniPHY-based Memory IP with SOPC Builder

A workaround is necessary to enable UniPHY-based memory IP support with SOPC Builder.

Affected Configurations

This issue affects all UniPHY-based designs with SOPC Builder.

Design Impact

The workaround is necessary or else the design fails.

Workaround

Perform the following steps to enable UniPHY-based memory IP support in SOPC Builder:

1. On the **Controller Settings** tab in the RLDram II Controller with UniPHY parameter editor, turn on **Generate power-of-2 data bus widths for SOPC Builder**.
2. On the **Controller Settings** tab in the RLDram II Controller with UniPHY parameter editor, turn on **Generate SOPC Builder compatible resets**.
3. After generating your external memory interface IP system, open your **.sopc** file in a text editor. In the **.sopc** file, locate lines similar to the following (where *<instance_name>* is the instance name of your IP core):

```
//reset sources mux, which is an e_mux
assign reset_n_sources = ~(~reset_n |
0 |
0 |
~<instance_name>_avl_resetrequest_n_from_sa |
~<instance_name>_avl_resetrequest_n_from_sa);
```

Replace each occurrence of *~<instance_name>_avl_resetrequest_n_from_sa* with 0 (zero), so that the above snippet becomes as follows:

```
//reset sources mux, which is an e_mux
assign reset_n_sources = ~(~reset_n |
0 |
0 |
0 |
0);
```

4. Manually reconnect the UniPHY reset inputs (*global_reset_n* and *soft_reset_n*) in the SOPC Builder-generated top-level file (*system.v*), as follows:

```
.global_reset_n (reset_n_sources),
.soft_reset_n (reset_n_sources),
```

Solution Status

This issue will not be fixed.

Using Avalon-MM Traffic Generator and BIST Engine

A workaround is necessary to enable the Avalon-MM Traffic Generator and BIST Engine.

Affected Configurations

This issue affects all UniPHY-based configurations using the Avalon-MM Traffic Generator and BIST Engine.

Design Impact

The workaround is necessary or else the Avalon-MM Traffic Generator and BIST Engine fails.

Workaround

Perform the following steps to enable the workaround:

1. On the **Controller Settings** tab in the RLDRAM II Controller with UniPHY parameter editor, turn on **Generate power-of-2 data bus widths for SOPC Builder**.
2. On the **Controller Settings** tab in the RLDRAM II Controller with UniPHY parameter editor, turn on **Generate SOPC Builder compatible results**.
3. Manually reconnect the reset input (reset_n) in the top-level file (system.v), as follows:

```
.reset_n (reset_n_sources),
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Simulation Fails when Generating VHDL for Designs Using Nios II-based Sequencer

For designs using the Nios II-based sequencer, simulation can fail when generating VHDL output.

Affected configurations

This issue affects designs using the Nios II-based sequencer and VHDL.

Design Impact

Simulation fails.

Workaround

The workaround for this issue requires that you manually modify certain files.

1. Look for three `.vhd` files with file names beginning with a string similar to the following:

`dut_dut_e0_if0_p0_qsys_sequencer_cpu_inst_jtag_debug_module` where `<dut>` is the name that you have specified for your project.

2. Open each of the three files in a text editor and add the following two lines to the beginning of each file:

```
library altera_mf;  
use altera_mf.altera_mf_components.all;
```

Solution Status

This issue will be fixed in a future version of the RLD RAM II Controller with UniPHY.

Cannot Share One PLL/DLL/OCT Master with Multiple Slaves in Qsys

The `alt_mem_if` interface supports the sharing of PLLs, DLLs, and OCTs using a sharing conduit; however, the conduit supports only point-to-point connections in Qsys, and therefore cannot be used to share a single master with multiple slaves.

Affected configurations

This limitation affects UniPHY-based designs built using Qsys.

Design Impact

The sharing of a single master with multiple slaves is not supported.

Workaround

There is no workaround for this limitation.

Solution Status

This issue will not be fixed.

Conduit Error Messages Displayed in Qsys

When generating a UniPHY-based IP core in Qsys, warning messages may appear stating that a given signal must be connected to a conduit. You may ignore such messages.

Affected configurations

This issue affects UniPHY-based designs generated with Qsys.

Design Impact

This issue has no design impact.

Workaround

Ignore the warning messages stating that a given signal must be connected to a conduit.

Solution Status

This issue will not be fixed.

Example Design Simulation May Fail in NC Sim

The autogenerated example design can fail during simulation in NC Sim.

Affected configurations

This issue affects all configurations.

Design Impact

This issue can cause the autogenerated example design to fail during simulation in NC Sim.

Workaround

Do not attempt to simulate the autogenerated example design in NC Sim.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Must Enable Support for Nios II ModelSim Flow in GUI

If you intend to use your generated IP with the **Run as Nios II ModelSim flow** in Eclipse, you must turn on the **Enable support for Nios II ModelSim flow in Eclipse** option on the **Diagnostics** tab in the parameter editor, or else your design may fail in Eclipse.

Affected configurations

This issue affects all designs targeting the ModelSim flow.

Design Impact

This issue can cause your design to fail in Eclipse.

Workaround

Ensure that you turn on the **Enable support for Nios II ModelSim flow in Eclipse** option on the **Diagnostics** tab in the parameter editor.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Simulation of Example Designs Can Fail or Produce Warnings

The example design for simulation may fail to compile or trigger compiler warnings in either the VCS or NC Sim simulators, if the simulation scripts are generated from NativeLink.

Affected Configurations

This issue affects all simulations of the generated example design.

Design Impact

Simulation in NC Sim or VCS may fail; other simulators may issue warning messages.

Workaround

The following workarounds apply to this issue:

- For simulation in VCS, add the `-debug_pp` option to the `.vcs` file generated by NativeLink.
- For simulation in NC Sim or any other simulator, remove the `$vcdpluson;` line from the `<variation_name>_example_design/simulation/<variation_name>_example_sim/submodules/status_checker.sv` file.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Compilation of a UniPHY Example Design Can Produce Warnings

If you compile a UniPHY-based example design in the Quartus II software, TimeQuest may produce warning messages similar to the following:

```
Warning: Ignored filter at altera_reset_controller.sdc (17):  
*|alt_rst_sync_up1|altera_rest_synchronizer_int_chain*|aclr could not  
be matched with a pin  
Warning: Ignored set_false_path at altera_reset_controller.sdc (17):  
Argument <from> is an empty collection
```

Affected Configurations

This issue affects all UniPHY-based example designs.

Design Impact

Warning messages are displayed.

Workaround

You may safely ignore these warning messages. To prevent these warning messages from appearing, you can modify the Qsys-generated Synopsys Design Constraints file `altera_reset_controller.sdc` so that the paths mentioned in the warnings conform to the specific hierarchy of your design. (Be aware that any changes that you make to the `.sdc` file might be overwritten if you regenerate your IP core.)

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

VHDL-only Simulation Not Supported

VHDL-only simulation is not supported in version 10.1 of the RLDRAM II Controller with UniPHY.

Affected Configurations

This issue affects all designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to use a mixed Verilog-VHDL simulator.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

When you specify VHDL output for the RLDRAM II Controller with UniPHY and attempt to simulate using NativeLink, NativeLink fails and reports that it cannot find the file *<design_name>.vho* in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to not use NativeLink for simulations of VHDL designs, but to set up simulation manually instead.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.0 of the Quartus II software, when a user specifies VHDL output for the RLDRAM II Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file `<design_name>.vho` in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to edit the `<design_name>.vhd` file and remove the line similar to the following:

```
-- IPFS_FILES : <design_name>.vho
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Timing-related Warning Messages When Sharing PLLs on Stratix V Devices

When instantiating a design in PLL/DLL slave mode on a Stratix V device, the TimeQuest Timing Analyzer may display warning messages similar to the following:

```
Warning: Ignored filter at slave_report_timing_core.tcl(176):  
slave_inst0|controller_phy_inst|memphy_top_inst|umemphy|uio_pads|  
dq_ddio[1].ubidir_dq_dqs|altdq_dqs2_inst|thechain|clkln could not be  
matched with a keeper or register or port or pin or cell or net  
  
Warning: Command get_path failed
```

Affected Configurations

This issue affects Stratix V designs instantiated in PLL/DLL slave mode.

Design Impact

The resulting timing analysis is incorrect.

Workaround

This issue has no workaround. The warning messages can be safely ignored; however, do not rely on the accuracy of the resulting timing analysis.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Reset Synchronizer May Cause Design to Fail Timing

Systems generated with SOPC Builder or Qsys may fail timing closure due to paths that include a reset synchronizer.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails timing closure.

Workaround

A workaround for this issue is to apply the following constraint in the TimeQuest Timing Analyzer:

For SOPC Builder:

```
set_false_path -from {dut_sopc_top_reset_clk_0_domain_synch_module:  
dut_sopc_top_reset_clk_0_domain_synch*}
```

For Qsys:

```
set_false_path -from *:rst_controller*|*:alt_rst_sync_uql|  
altera_reset_synchronizer_int_chain[*] -to *:controller_phy_inst|  
*:memphy_top_inst|*:umemphy|*:ureset|*:ureset_*_clk|reset_reg[*]
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Compilation Fails if Synthesis Fileset is Mixed with Example Project Files

Compilation fails if the **Files** list in the **Settings** dialog box in the Quartus II software includes files from both the example project located at `<working_dir>/<variation_name>_example_design_fileset/example_project/` and the synthesis fileset located at `<working_dir>/<variation_name>`.

Affected Configurations

This issue affects all configurations.

Design Impact

Compilation fails.

Workaround

A workaround for this issue is to perform the following steps:

1. In an editor, open the `<variation_name>_driver.sv` file, located in the `<working_dir>/<variation_name>_example_design_fileset/example_project/` directory.

2. In the `<variation_name>_driver.sv` file, change the entity name `<variation_name>_reset_sync` to `<variation_name>_<num>_reset_sync`, where *num* is the same value as in the `<variation_name>_<num>_reset_sync.v` filename in the `<working_dir>/<variation_name>/` directory.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Warning Messages Displayed When Compiling for Stratix V Devices

When compiling a design for Stratix V devices, the system may display numerous PLL-related warning messages similar to the following:

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 do not have a PLL clock to compensate specified - the Fitter will attempt to compensate all PLL

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 use multiple different clock network types - the PLL will compensate for output clocks

Warning: PLL cross checking found inconsistent PLL clock settings:

Warning: Node: mem_if|controller_phy_inst|memphy_top_inst|pll1~FRACTIONAL_PLL|mcntout was found missing 1 generated clock that corresponds to a base clock with a period of: 8.000

Warning: Clock: mem_if|ddr3_pll_write_clk was found on node: mem_if|controller_phy_inst|memphy_top_inst|pll3|outclk with settings that do not match the following PLL specifications:

Warning: -multiply_by (expected: 21, found: 4264000)

Warning: -divide_by (expected: 5, found: 1000000)

Warning: -phase (expected: 0.00, found: 90.00)

These warning messages are expected and can be ignored.

Affected Configurations

This issue affects all configurations targeting Stratix V devices.

Design Impact

This issue has no design impact.

Workaround

There is no workaround for this issue. You can safely ignore the error messages.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Cannot Launch MegaWizard Plug-In Manager by Opening Example Design

You cannot reopen your project in the MegaWizard Plug-In Manager by clicking on your generated IP instantiation

`<working_dir>/<variation_name>_example_design/example_project/`

`<variation_name>_example/<variation_name>_example.v`

or

`<working_dir>/<variation_name>_example_design/simulation/<variation_name>_`

`example_sim/<variation_name>_example_sim.v`

Affected configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

To reopen your variation in the MegaWizard Plug-In Manager, follow these steps:

1. In the Quartus II software, click **MegaWizard Plug-In Manager** on the **Tools** menu.
2. Click **Edit an existing custom megafunction variation** and specify:
`<working_dir>/<variation_name>.v`.

Solution Status

This issue will not be fixed.

Example Design May Not Compile for IP Cores from Earlier Versions

The example design provided with version 10.1 may not compile with IP cores migrated from earlier versions of the Quartus II software.

Affected configurations

This issue affects all configurations.

Design Impact

Attempting to compile the example design with IP cores migrated from earlier versions of the Quartus II software may fail with the following message:

Error:instance "ureset_driver_clk" instantiates undefined entity
"<variation_name>_reset_sync"

Workaround

The workaround for this issue is to perform the following steps:

1. In the Quartus II software, open the **Settings** dialog box on the **Assignments** menu.
2. In the **Category** tree of the **Settings** dialog box, click **Files** to display the files list.

3. Remove all the UniPHY files, including the **.qip** file and example project files, from the migrated project assignments.
4. Add to the project the newly generated **.qip** file located in the `<working_dir>/<variation_name>_example_design_fileset` directory.
5. Add to the project all of the files except for the memory model, from the directory `<working_dir>/<variation_name>_example_design_fileset/example_project`.

Solution Status

This issue will be fixed in a future version of the RLD RAM II Controller with UniPHY.

Calibration Failure in Earlier Versions

Designs generated in version 10.0SP1 and earlier may experience calibration failure due to unreliable asynchronous signal transfer from the AFI clock domain to the read-capture clock domain.

Affected Configurations

This issue affects full-rate IP cores generated in version 10.0SP1 and earlier of the RLD RAM II Controller with UniPHY.

Design Impact

Designs fail in calibration.

Workaround

Open the design in version 10.1 of the RLD RAM II Controller with UniPHY and regenerate the design.

Solution Status

This issue is fixed in version 10.1 of the RLD RAM II Controller with UniPHY.

SOPC Builder-generated Systems Cannot Serve as Top-Level Design

Systems generated with SOPC Builder cannot serve as the top-level design, because SOPC Builder automatically exports the `parallelterminationcontrol` and `seriesterminationcontrol` OCT control signals as top-level ports, but these signals must not be exposed at the top level.

Affected configurations

This issue affects all configurations generated with SOPC Builder.

Design Impact

Compilation fails.

Workaround

Perform either of the following procedures to work around this issue:

- Create a top-level wrapper which instantiates the SOPC Builder-generated system, and does not make any connection to the `parallelterminationcontrol` or `seriesterminationcontrol` signals.

or

- Open the top-level SOPC Builder system file (for example, *system.v*), and delete the wire names from within the brackets for the `parallelterminationcontrol` and `seriesterminationcontrol` signals for all UniPHY cores. The resulting lines should appear as follows:

```
.parallelterminationcontrol ()  
.seriesterminationcontrol ()
```

The wire names that you delete from within the brackets must also be removed from all other locations in the top-level system file, including the top-level port list.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices

In Stratix V devices, the corner I/O banks are expected to have higher core-to-I/O and I/O-to-core delay and skew values than the other I/O banks, and are unsuitable for interfacing with external memory at frequencies above 667 MHz.

The characteristics of the corner I/O banks are not yet reflected in the Stratix V timing models available in version 10.1 of the Quartus II software; consequently, timing analysis will not accurately characterize the performance of the corner I/Os.

Affected Configurations

This issue affects all configurations targeting Stratix V devices at frequencies above 667 MHz.

Design Impact

This issue can adversely affect timing.

Workaround

Avoid using the outer I/O banks at the upper and lower sides of the device.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Simulation Fails—PLL Clocks Out of Synchronization

During simulation, the PLL clocks lose synchronization.

Affected Configurations

This issue affects all designs.

Design Impact

This issue causes simulation failures.

Workaround

To work around this issue, follow these steps:

1. In text editor open the design file and remove the following line:

```
coverage exclude_file
```
2. In the ALTPLL MegaWizard interface, turn on **Create output files using the Advanced PLL parameters** and regenerate the PLL ().

Selecting VHDL Gives a Verilog HDL IP Core

If you select VHDL in the MegaWizard interface and generate an RLDram II controller with UniPHY IP core, the generated core is in Verilog HDL.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The issue affects all VHDL designs.

Workaround

To generate a VHDL IP core follow these steps:

1. In a text editor open
`<Quartus II directory>\ip\altera\uniphy\lib\altera_uniphy_rldramii_hw.tcl.`
2. Search for the string "LANGUAGE" that appears in the following code:

```
append param_str ",LANGUAGE=[get_generation_property HDL_LANGUAGE]"
```
3. Change this line to the following code:

```
append param_str ",LANGUAGE=vhdl"
```
4. Continue searching for the next occurrence of the string "LANGUAGE" which appears in the following code:

```
if {[string compare -nocase [get_generation_property HDL_LANGUAGE]  
verilog] == 0} {  
    add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}  
    puts $qipfile "set_global_assignment -name VERILOG_FILE \[file  
join \${::quartus(qip_path) ${outputname}.v\]"  
} else {
```

```

        add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}

        puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\${::quartus(qip_path) ${outputname}.vhd\"]"
    }

```

5. Comment out the if line, the else line, and the block of code in the conditional section so that the code in the "else" block always executes, similar to the following code:

```

# if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
#     add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
#     puts $qipfile "set_global_assignment -name VERILOG_FILE \[file join
join \${::quartus(qip_path) ${outputname}.v\"]"
# } else {
    add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
    puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\${::quartus(qip_path) ${outputname}.vhd\"]"
# }

```

6. Use the MegaWizard interface to generate a UniPHY-based IP core.



To generate a Verilog HDL IP core, restore the original **altera_uniphy_rldramii_hw.tcl** file.

Solution Status

This issue will be fixed in a future version of the RLD RAM II Controller with UniPHY IP core.

Incorrect Clock Uncertainty

A clock uncertainty related to the read FIFO clocked by DQS can result in inaccurate setup and hold slack values. The solution described in the 15 July 2010 version of the MegaCore IP Library Release Notes and Errata contained an error which this solution corrects.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can cause setup and hold slack values to be inaccurate.

Workaround

The workaround for this issue is to manually edit the PHY **.sdc** file located in the `<variation_name>/constraints/` directory, and add the following two lines to the Multicycle Constraints section of the file:

```

set_max_delay -from *ddio_in_inst_regout* -0.05
set_min_delay -from *ddio_in_inst_regout* [expr -$t(CK) + 0.05]

```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

BSF File Not Generated

The IP core does not generate a BSF file, and therefore is not compatible with workflows requiring a BSF file.

Affected Configurations

This issue affects all configurations.

Design Impact

Errors are likely to occur with workflows using the Schematic Editor or Symbol Editor.

Workaround

Do not use the Schematic Editor or the Symbol Editor with the IP core.

Solution Status

This issue is fixed in version 10.1 of the RLDRAM II Controller with UniPHY.

Global Signal Assignments Not Applied

The Fitter sometimes does not honor GLOBAL signal assignments applied by the `<variation_name>_pin_assignments.tcl` script.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no impact on the correctness of the design, but can result in suboptimal resource placement and can contribute to difficulties in achieving timing closure.

Workaround

To determine whether GLOBAL assignments are properly applied, check the Fitter Report and verify whether any GLOBAL signal assignment referring to a PLL output port (for example, `...|auto_generated|clk[*]`) appears in the **Ignored Assignments** section.

If there is a GLOBAL assignment to a PLL output port listed in **Ignored Assignments**, you can correct the problem by running Analysis & Synthesis and then running the Fitter. You should then verify in the Fitter Report that the assignment is no longer ignored.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

UniPHY DQS Clock Buffer Location

The DQS clock buffer location for the UniPHY can cause hold time violations when placed suboptimally. The Quartus II software may suboptimally place the DQS clock buffer on a global or dual-regional clock after reentering the FPGA, so that it can be routed to the write side of the read capture FIFO.

Affected Configurations

The issue affects all configurations.

Design Impact

You may see hold time failures on the capture clocks in core logic.

Workaround

Create a location assignment on the buffer to the same edge as the memory interface (for example `EDGE_BOTTOM`).

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

IP Functional Simulation Model

The wizard-generated IP core functional simulation model (`.vho`) file for VHDL designs is functionally incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use an IP core functional simulation model to simulate your design.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the RLDRAM II Controller with UniPHY.

No Link to User Guide from Wizard

The wizard does not have a link to the [RLDRAM II Controller with UniPHY User Guide](#).

Affected Configurations

The issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Access the *RLDRAM II Controller with UniPHY User Guide* from the Altera website.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

-18 Presets Give Errors

If you select any preset with -18 (for example, MT49H64M9-18, MT49H32M18-18, MT49H16M36-18), you see the following error:

```
Error: <variation>: Memory clock frequency must be between 170 MHz  
and 500 MHz
```

Affected Configurations

The issue affects all -18 presets.

Design Impact

If you select a 533-MHz component, the FPGA device fails to meet timing.

Workaround

Ensure you change the frequency to a supported frequency.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Revision History

Table 29–1 shows the revision history for the SDI MegaCore function.



For more information about the new features, refer to the *SDI MegaCore Function User Guide*.

Table 29–1. SDI MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> ■ Preliminary support for Stratix V devices. ■ Final support for Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. ■ Added new 8-bit video format output features for receiver and duplex instances. ■ Added unencrypted ALTGX wrapper file. ■ Added incoming video data rate indicator. ■ Removed Enable Spread Spectrum feature.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> ■ Preliminary support for Arria II GZ devices. ■ Final support for Arria II GX and Stratix IV GT devices. ■ Added new GUI parameter: Enable Spread Spectrum feature.
10.0 SP1	September 2010	Added new GUI parameter: Tolerance to consecutive missed EAV .
10.0	July 2010	Added DPRIO with PLL Reconfiguration mode for Cyclone IV GX devices.

Errata

Table 29–2 shows the issues that affect the SDI MegaCore function v11.0, 10.1, and 10.0.



Not all issues affect all versions of the SDI MegaCore function.

Table 29-2. SDI MegaCore Function Errata

Added or Updated	Issue	Affected Version			
		11.0	10.1 SP1	10.1	10.0
1 Jul 11	SDI MegaCore Function Fails to Launch in Windows	✓	—	—	—
	Designs Targeting Stratix V Fail Reconfiguration	✓	—	—	—
	SDI Audio Embed MegaCore Function Samples Wrong Audio Data	✓	✓	✓	—
	Embedded Audio Signal Not Stable	✓	✓	✓	—
	Missing Control Packet for the First Audio Group	✓	✓	✓	—
	SDI Audio Extract MegaCore Function Shows Incorrect Behavior	✓	✓	✓	—
	Audio Clock Contains High Jitter	✓	✓	✓	—
15 May 11	Designs Targeting Stratix V Fail to Generate Simulation Model	✓	—	—	—
	SDI Audio MegaCore Function Designs with SOPC Builder Fail to Generate	Fixed	✓	—	—
	SDI Audio MegaCore Function Designs with SOPC Builder or Qsys Fail to Generate	Fixed	✓	—	—
	Receiver Operation Mode Does Not Support Spread Spectrum Clocking Feature	—	✓	—	—
15 Feb 11	Duplex Operation Mode Does Not Support Spread Spectrum Clocking Feature	—	✓	—	—
	HD-SDI Dual Link RX Data Misalign When Cable Connection is Interrupted	—	Fixed	✓	✓
	rx_status Signal Not Reliable in HD-SDI Dual Link Receiver	—	Fixed	✓	✓
15 Dec 10	The Quartus II Fitter Reports Error When Separate TX and Duplex TX Are Assigned in the Same Transceiver Quad	✓	✓	✓	—
15 July 10	Pulse Width Violation in TimeQuest Report	✓	✓	✓	✓
01 Apr 10	Quartus II Fitter Reports Error When Multiple Channels in One Transceiver Quad Use More than One Reference Clock	✓	✓	✓	✓
15 Nov 09	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓	✓
01 Nov 08	Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices	✓	✓	✓	✓
15 May 08	NativeLink Fails With ModelSim Simulator	✓	✓	✓	✓
01 Mar 08	Timing Not Met in C5 Speed Grade Stratix II GX Devices	✓	✓	✓	✓

SDI MegaCore Function Fails to Launch in Windows

The SDI MegaCore function version 11.0 fails to launch in Windows if the installation path for the Windows-platform ACDS contains spaces.

Affected Configurations

This issue affects all SDI IP cores.

Design Impact

You cannot access the SDI parameters through the MegaWizard Plug-In Manager.

Workaround

Install the ACDS Suite in a directory that does not contain spaces in its path.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Designs Targeting Stratix V Fail Reconfiguration

SDI designs targeting Stratix V devices fail reconfiguration with the transceiver dynamic reconfiguration controller.

Affected Configurations

This issue affects all SDI configurations that target a Stratix V device.

Design Impact

The design may fail to work in hardware.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

SDI Audio Embed MegaCore Function Samples Wrong Audio Data

The SDI Audio Embed MegaCore Function supports both synchronous and asynchronous mode, but the embed audio IP core is internally preset as synchronous mode only. If you connect the `aud_clk` signal for the SDI Embed Audio IP core to any frequency other than 3.072 MHz, the core may sample the audio data wrongly and the oscilloscope detects the audio data as mute.

Affected Configurations

This issue affects all SDI Audio Embed IP core configurations.

Design Impact

The design may sample the audio data wrongly.

Workaround

To enable the asynchronous mode, open the generated `<variation_name>.v` file and add the following line:

```
.G_AUDEMB_INPUT_ASYNC (1)
```

To enable back to synchronous mode, open the generated `<variation_name>.v` file and change (1) to (0):

```
.G_AUDEMB_INPUT_ASYNC (0)
```

Solution Status

This issue will be fixed in a future version of the SDI Audio Embed MegaCore function.

Embedded Audio Signal Not Stable

When you transmit an embedded audio in an SDI instance, the embedded audio detected switches repeatedly between locked and unlocked. The AES input module causes the embedded audio signal to be unstable.

Affected Configurations

This issue affects all SDI Audio Embed configurations that use the AES input module.

Design Impact

The embedded audio in the video signal may not be stable.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the SDI Audio Embed MegaCore function.

Missing Control Packet for the First Audio Group

When SDI MegaCore function transmits the embedded audio signal in 3G-SDI level B video standard, the oscilloscope does not detect the control packet for the first audio group.

Affected Configurations

This issue affects all SDI Audio Embed configurations in 3G-SDI level B video standard.

Design Impact

The control packet for the first audio is not detected.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the SDI Audio Embed MegaCore function.

SDI Audio Extract MegaCore Function Shows Incorrect Behavior

The SDI Audio Extract MegaCore function shows incorrect behavior when extracting the audio signal embedded in SD-SDI video format.

Affected Configurations

This issue affects all SDI Audio Extract configurations in SD-SDI video standard.

Design Impact

The extracted audio signal may be incorrect.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the SDI Audio Extract MegaCore function.

Audio Clock Contains High Jitter

The audio clock, `aud_clk_out`, generated by the SDI Audio Extract MegaCore function contains high jitter. The SDI Audio Extract MegaCore function generates `aud_clk_out` at a frequency of 3.072 MHz, that is synchronous to the receiving video data, but contains high jitter.

Affected Configurations

This issue affects all SDI Audio Extract configurations.

Design Impact

The generated audio signal contains high jitter.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the SDI Audio Extract MegaCore function.

Designs Targeting Stratix V Fail to Generate Simulation Model

Designs that use the SDI MegaCore function targeting a Stratix V device fail to generate a simulation model in MegaWizard Plug-In Manager.

Affected Configurations

This issue affects all SDI configurations that target a Stratix V device.

Design Impact

The MegaWizard Plug-In Manager fails to generate the simulation model and shows the following error messages:

```
"Error: Node instance "transceiver_core" instantiates undefined entity
"sv_xcvr_custom_native"

>Error:<proj_name>:HDL Generation Failed"
```

Workaround

To generate a simulation model for your Stratix V design, follow these steps:

1. In the Quartus II software, create a project and launch the MegaWizard Plug-In Manager.
2. Create a new custom megafunction variation, and select the desired SDI configuration
3. On the **EDA** tab, make sure to turn off **Generate simulation model**.
4. Click **OK**.
5. In a command terminal, change the directory to the project folder to generate **xcvr** and **sdi-library** folders.
6. Run the **quartus_map** script as follows:

- a. Verilog Example:

```
quartus_map <proj_name>.v --simgen --simgen_parameter="CBX_HDL_LANGUAGE=Verilog"
--family="Stratix V"
```

- b. VHDL Example:

```
quartus_map <proj_name>.vhd --simgen --simgen_parameter="CBX_HDL_LANGUAGE=Vhdl"
--family="Stratix V"
```

7. The **<proj_name>.vo** or **vho** file gets generated at the project directory.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

SDI Audio MegaCore Function Designs with SOPC Builder Fail to Generate

If you create an SOPC Builder design using any of the SDI Audio MegaCore functions, your design fails to generate and shows the following error:

```
Node instance "<sdi_audio_core_name>_0" instantiates undefined entity
"<sdi_audio_core_name>"
```

Affected Configurations

This issue affects all designs that use any of the SDI Audio MegaCore functions—Audio Embed, Audio Extract, Clocked Audio Input, Clocked Audio Output—in SOPC Builder.

Design Impact

The design fails to generate in SOPC Builder.

Workaround

To generate SDI Audio MegaCore functions in SOPC Builder, follow these steps:

1. Open a text editor and type the following commands

```
<QUARTUS_ROOTDIR>\ip\altera\<sdi_audio_core_name>\src\<sdi_audio_core_name>_hw.tcl
```

2. Remove the following line:

```
package require -exact soc 10.0
```



Replace `<sdi_audio_core_name>` with `audio_embed`, `audio_extract`, `clocked_audio_input` or `clocked_audio_output`.

Solution Status

This issue is fixed in version 11.0 of the SDI MegaCore function.

SDI Audio MegaCore Function Designs with SOPC Builder or Qsys Fail to Generate

If you create an SOPC Builder or Qsys design using any of the SDI Audio MegaCore functions, your design fails to generate and shows the following error:

```
Overwriting different file  
/myproject/synthesis/submodules/altera_reset_synchronizer.v
```

Affected Configurations

This issue affects all designs that use any of the SDI Audio MegaCore functions—Audio Embed, Audio Extract, Clocked Audio Input, Clocked Audio Output—in SOPC Builder.

Design Impact

The design fails to generate in SOPC Builder or Qsys.

Workaround

To generate SDI Audio MegaCore functions in SOPC Builder or Qsys, follow these steps:

1. Open a text editor and type the following commands

```
<QUARTUS_ROOTDIR>\ip\altera\<sdi_audio_core_name>\src\<sdi_audio_core_name>_hw.tcl
```

2. Remove the following line:

```
"add_file ${module_dir}/../verilog/altera_reset_synchronizer.v  
{SYNTHESIS}
```



Replace `<sdi_audio_core_name>` with `audio_embed`, `audio_extract`, `clocked_audio_input` or `clocked_audio_output`.

Solution Status

This issue is fixed in version 11.0 of the SDI MegaCore function.

Receiver Operation Mode Does Not Support Spread Spectrum Clocking Feature

Designs targeting some Cyclone IV GX devices in receiver operation mode and with the **Enable Spread Spectrum** option turned on may fail to compile.

Affected Configurations

This issue affects all designs targeting Cyclone IV GX devices—EP4CGX30 (F484), EP4CGX50, and EP4CGX75—with the **Enable Spread Spectrum feature** option turned on.

Design Impact

The design fails to compile.

Workaround

None.

Solution Status

The Enable Spread Spectrum feature is removed from the 11.0 version of the SDI MegaCore function.

Duplex Operation Mode Does Not Support Spread Spectrum Clocking Feature

Designs targeting some Cyclone IV GX devices in duplex operation mode and with the **Enable Spread Spectrum** option turned on may fail to compile.

Affected Configurations

This issue affects all designs targeting Cyclone IV GX devices—EP4CGX30 (F484), EP4CGX50, and EP4CGX75—with the **Enable Spread Spectrum feature** option turned on.

Design Impact

The design fails to compile.

Workaround

Use separate SDI RX and TX instances if your design requires the spread spectrum clocking feature.

Solution Status

The Enable Spread Spectrum feature is removed from the 11.0 version of the SDI MegaCore function.

HD-SDI Dual Link RX Data Misalign When Cable Connection is Interrupted

The rx data from the HD-SDI dual link is not synchronized if either Link A or Link B's BNC cable connection is interrupted. When the rxdata is misaligned, the rx_status[10] signal remains high.

Affected Configurations

This issue affects all HD-SDI dual link receiver configurations.

Design Impact

HD-SDI Link A data (rxdata[19:0]) misalign with HD-SDI Link B data (rxdata[39:20])

Workaround

Apply hardware reset to the SDI MegaCore function if the cable connection is interrupted.

Solution Status

This issue is fixed in version 10.1 SP1 of the SDI MegaCore function.

rx_status Signal Not Reliable in HD-SDI Dual Link Receiver

The rx_status[10] signal is not reliable in the HD-SDI dual link receiver core if two incoming streams are synchronized ahead of the reception.

Affected Configurations

This issue affects all HD-SDI dual link receiver configurations.

Design Impact

The rx_status[10] signal toggles.

Workaround

None.

Solution Status

This issue fixed in version 10.1 SP1 of the SDI MegaCore function.

The Quartus II Fitter Reports Error When Separate TX and Duplex TX Are Assigned in the Same Transceiver Quad

For designs with the **Enable PLL Reconfiguration** option turned on and targeting Cyclone IV GX devices, the Quartus II Fitter reports an error when separate TX and duplex TX SDI instances are assigned in the same transceiver quad.

Affected Configurations

This issue affects all designs targeting Cyclone IV GX devices with the **Enable PLL Reconfiguration** option turned on.

Design Impact

The design cannot be fitted in the device.

Workaround

Uses separate RX and TX SDI instances to fit more than 1 SDI transmitter in a transceiver quad.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Pulse Width Violation in TimeQuest Report

The TimeQuest report may show minimum pulse width violation when you run full compilation on a soft-SERDES design.

Affected Configurations

This issue affects all soft-SERDES designs.

Design Impact

Your design does not meet the timing requirements.

Workaround

Specify the I/O standard for the clock pins so that the clock pins perform better and runs with a higher speed. For example, if you see pulse width violation on the rx_serial_clk and rx_serial_clk90 clock inputs, in the .qsf file add the following commands:

```
set_instance_assignment -name IO_STANDARD LVCMOS -to rx_serial_clk  
set_instance_assignment -name IO_STANDARD LVCMOS -to rx_serial_clk90
```

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Quartus II Fitter Reports Error When Multiple Channels in One Transceiver Quad Use More than One Reference Clock

The Quartus II Fitter reports an error when multiple channels within one transceiver quad use more than one reference clock in Stratix II GX devices.

For example, four SDI transmitter core is instantiated four times for 4 video channels. These four channels reside within one transceiver quad of a Stratix II GX device. There are two reference clocks connected to this quad—two channels use the first reference clock, and the other two use the second reference clock.

Affected Configurations

This issue affects all designs targeting Stratix II GX devices.

Design Impact

The design cannot be fitted in the device.

Workaround

Apply the quartus variable in the design, by doing the following steps:

1. Create a **quartus.ini** file with content
farm_s2gx_dprio_bypass_pll_number_check=on.
2. Place the **quartus.ini** file you created in your design folder, and compile the design in the Quartus II software version 9.1 SP2.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

The Quartus II Design Assistant Reports Critical Warning

When the **rx_protocol_clk** clock is used, the Quartus II Design Assistant reports the following error:

"Critical Warning: (High) Rule D103: Data bits are not correctly synchronized when transferred between asynchronous clock domains."

This clock is not constrained in the SDC file.

Affected Configurations

This issue affects the dual link SDI in split protocol mode.

Design Impact

The design may fail to function properly on the hardware.

Workaround

Add the following constraints into the SDC file:

```
set rx_protocol_clk_name "rx_protocol_clk[1]"  
  
create_clock -name $rx_protocol_clk_name -period 13.468 -waveform {0.000 6.734}  
[get_ports $rx_protocol_clk_name]
```

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices

The Quartus II Fitter reports an error when you use PLL-generated clock inputs of 67.5 MHz frequency in SDI-SD MegaCore targeting Stratix GX devices.

Affected Configurations

This issue affects all Stratix GX SDI-SD MegaCore functions with PLL-generated clock inputs of 67.5 MHz frequency.

Design Impact

The design cannot be fitted in the device.

Workaround

Set the input clock to 29.7 MHz frequency so that the PLL generates the frequency of the output clock to 74.25 MHz.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

NativeLink Fails With ModelSim Simulator

When using NativeLink to run simulations with the ModelSim simulator, the testbench fails.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate and the testbench reports a failure.

Workaround

Use the ModelSim simulation scripts provided by Altera or carry out the following steps:

1. Edit the NativeLink generated script to command
"vsim -t 100fs".
2. Reexecute the script in ModelSim.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Timing Not Met in C5 Speed Grade Stratix II GX Devices

The 3-Gbps and triple rate variants of the SDI MegaCore function may not meet the timing requirements in the C5 speed grade device of the Stratix II GX device family.

Affected Configurations

This issue affects the 3-Gbps and triple-rate SDI MegaCore functions.

Design Impact

Your design does not meet timing requirements.

Workaround

Use either a C4 or C3 speed grade device.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Revision History

Table 30–1 shows the revision history for the SerialLite II MegaCore function.



For more information about the new features, refer to the *SerialLite II MegaCore Function User Guide*.

Table 30–1. SerialLite II MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	Maintenance release.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	Final support for Arria II GX and Stratix IV GT devices.
10.0	July 2010	Maintenance release.

Errata

Table 30–2 shows the issues that affect the SerialLite II MegaCore v11.0, 10.1, and 10.0.



Not all issues affect all versions of the SerialLite II MegaCore.

Table 30–2. SerialLite II MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	The Quartus II Software Indicates Support for Arria II GX as Preliminary	Fixed	✓	✓
15 Nov 09	Designs with Frequency Offset Tolerance Enabled Fail Testbench Simulation	✓	✓	✓
	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓

The Quartus II Software Indicates Support for Arria II GX as Preliminary

The Quartus II software version 10.1 issues an incorrect warning indicating that the support for Arria II GX devices is preliminary. The Arria II GX support for the SerialLite II MegaCore function is final.

Affected Configurations

This issue affects all configurations.

Design Impact

None.

Workaround

Ignore the warning.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Designs with Frequency Offset Tolerance Enabled Fail Testbench Simulation

Designs that have the **Frequency Offset Tolerance** option turned on to either 100 ppm or 300 ppm, using streaming or packet mode with an RX buffer size of zero with a non-default reference clock frequency, may fail the demonstration testbench simulation citing data mismatch errors.

This issue occurs because the utilities for the testbench monitor run at a different clock rate compared to the DUT's receive side's Atlantic clock rate.

Affected Configurations

This issue affects designs with the following settings:

- **Frequency Offset Tolerance** turned on to either 100 ppm or 300 ppm
- Streaming mode or Packet mode with RX buffer size = 0
- Reference clock frequency not equal to $(\text{data rate}/(\text{TSIZE} \times 10))$

Design Impact

There is no design impact. This is a demonstration testbench issue.

Workaround

To simulate the testbench successfully, perform the following steps:

1. Open the generated **<design>_tb.v**.
2. Search for the instantiation of **amon_dat_dut**, and replace the **trefclk** in the clock connection with **tx_coreclock**.

For example,

Original line: `.clk (trefclk & reset_done)`

Replaced line: `.clk(tx_coreclock & reset_done)`

3. Repeat step 2 for **amon_dat_sis**, **amon_pri_dut**, and **amon_pri_sis** (if you have enabled Priority Port).
4. Search for the instantiation of **sbrd_dat_dut_to_sis**, and replace the **trefclk** in the **rclk** connection with **tx_coreclock**:

For example,

Original line: `,.rclk (trefclk)`

Replaced line: `,.rclk (tx_coreclock)`

5. Repeat step 4 for **sbrd_pri_dut_to_sis**, **sbrd_dat_sis_to_dut**, and **sbrd_pri_sis_to_dut**.

Solution Status

This issue will be fixed in a future version of the SerialLite II MegaCore function.

The Quartus II Design Assistant Reports Critical Warning

When you compile a SerialLite II design that targets Stratix GX devices, the Quartus II Design Assistant reports the following error:

```
Critical Warning: (Critical) Rule C101: Gated clock should be  
implemented according to the Altera standard scheme. Found 1 node(s)  
related to this rule.
```

```
    Critical Warning: Node  
    "<design>_slite2_top|slite2_top_inst|slite2_xcvr:xcvr_inst|altgxb:altg  
    xb_component|rx_clkout_wire[0]
```

This warning, if targeted to the rx_clkout_wire[0], is erroneously issued by the Quartus II Design Assistant, and is not valid. You can ignore this warning.

Affected Configurations

This issue affects all designs that target Stratix GX devices.

Design Impact

There is no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Revision History

Table 31–1 shows the revision history for the Stratix V Hard IP for PCI Express.



For more information about the new features, refer to the *Stratix V Hard IP for PCI Express User Guide*.

Table 31–1. Stratix V Hard IP for PCI Express Revision History

Date	Version	Description
July 2011	11.0 SP1	Maintenance Release
May 2011	11.0	First release.

Errata

Table 31–2 shows the issues that affect the Stratix V Hard IP for PCI Express v11.0 and 11.0 SP1.



Not all issues affect all versions of the Stratix V Hard IP for PCI Express.

Table 31–2. Stratix V Hard IP for PCI Express Errata

Added or Updated	Issue	Affected Versions	
		11.0 SP1	11.0
15 July 11	Root Port Bus Functional Model (BFM) and Endpoint Design Example Not Available	✓	—
1 July 11	Top-Level Stratix V PCI Express Module Includes derr_cor_ext_rcv1	Fixed	✓
15 May 11	Error in Getting Started Instructions for Post-Compilation Simulation	✓	✓

Root Port Bus Functional Model (BFM) and Endpoint Design Example Not Available

The root port BFM and endpoint design example are not available for simulation in version 11.0 SP1 of the Quartus II software. If you begin simulation, the following message displays, “BFM model not available.”

Affected Configurations

This issue affects the root port and endpoint design examples described in the “Testbench and Design Example” chapter of the *Stratix V Hard IP for PCI Express User Guide*.

Workaround

The workaround is to use a third-party BFM for simulation.

Solution Status

For the 11.0 SP1 release, the solution is to purchase a third-party BFM.

Top-Level Stratix V PCI Express Module Includes derr_cor_ext_rcv1

The top-level Verilog HDL module for the PCI Express IP core includes the `derr_cor_ext_rcv1` signal; however, this signal is not required or functional for Stratix V devices.

Affected Configurations

This issue affects all configurations of the Stratix V Hard IP for PCI Express.

Workaround

After generating your Stratix V Hard IP for PCI Express, remove `derr_cor_ext_rcv1` from the `<pcie_variant>.v`.

Solution Status

This issue is fixed in version 11.0 SP1 of the Stratix V Hard IP for PCI Express.

Error in Getting Started Instructions for Post-Compilation Simulation

The “Compile the Design in the Qsys Design Flow” section in the “Getting Started” chapter of the *Stratix V Hard IP for PCI Express User Guide* incorrectly instructs you to select **ModelSim** for the **Simulation** on the **EDA Toll Settings** page. This step causes the Quartus II software to try to create a post-simulation netlist; however, post-compilation netlist generation is not supported.

Affected Configurations

This is a documentation error only.

Workaround

When creating your Quartus II project, do not select a simulation tool on the **EDA Tool Settings** page.

Solution Status

This issue will be fixed in a future version of the *Stratix V Hard IP for PCI Express User Guide*.

Revision History

Table 32–1 shows the revision history for the Triple Speed Ethernet MegaCore function.



For more information about the new features, refer to the *Triple Speed Ethernet MegaCore Function User Guide*.

Table 32–1. Triple Speed Ethernet MegaCore Function Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Cyclone IV GX, Cyclone III LS, Arria II GZ, HardCopy III E and HardCopy IV E/GX devices.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Added a new parameter, Starting Channel Number.
10.0	July 2010	Preliminary support for Stratix V devices.

Errata

Table 32–2 shows the issues that affect the Triple Speed Ethernet MegaCore function v11.0, v10.1, and v10.0.



Not all issues affect all versions of the Triple Speed Ethernet MegaCore function.

Table 32–2. Triple Speed Ethernet MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
1 Jul 11	Auto-Negotiation Could Not Complete in 1000BASE-X PCS Function	✓	✓	✓
	Warning Messages for Stratix V Designs	✓	—	—
	Simulation Fails for Stratix V Designs Instantiated Using SOPC Builder	✓	—	—
	Unconstraint Clock in Stratix V Designs with GXB Transceiver and Transceiver Reconfiguration Controller Megafunction	✓	—	—
	Timing Not Met in Stratix V Devices	✓	—	—
	Critical Warning Message for Stratix V Devices	✓	—	—
	Critical Warning Messages for 1000BASE-X/SGMII PCS Functions	✓	—	—
	Critical Warning Messages When Local Loopback is Enabled	✓	—	—
15 May 11	Critical Warning Message for HardCopy Devices	✓	—	—
	Fitter Error for Cyclone IV GX Devices with 1000BASE-X/SGMII PCS Functions	Fixed	✓	—

Table 32–2. Triple Speed Ethernet MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 Mar 11	Late Collision in Half-Duplex 10/100-Mbps Ethernet MAC	Fixed	✓	✓
	Packet Loss in 8-bit Internal FIFO Buffer	Fixed	✓	✓
	Speed Change Causes Corrupt Packet	Fixed	✓	✓
	Statistics Counters Issues	Fixed	✓	✓
	Continuous Data Transmission from MAC Function	Fixed	✓	✓
	Half-Duplex Mode Post Collision Issues	Fixed	✓	✓
	Transceiver Quad Sharing Failure	Fixed	✓	✓
	PLL Sharing Problem for LVDS Channels	Fixed	✓	✓
	Reset Synchronization Problem	Fixed	✓	✓
	MII Local Loopback Failure	Fixed	✓	✓
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—
15 Dec 10	Simulation Fails for HardCopy IV GX with GXB Transceiver	✓	✓	✓
15 Sep 10	Corrupted Packets in 10/100-Mbps Designs with GXB Transceiver	Fixed	Fixed	✓
15 July 10	Unstable Designs with LVDS in Hardware	✓	✓	✓
15 Mar 09	Timing Not Met in Cyclone III Devices	✓	✓	✓
15 May 08	Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register	✓	✓	✓
	Non-Compliant Implementation of aAlignmentError Statistics Counter	✓	✓	✓

Auto-Negotiation Could Not Complete in 1000BASE-X PCS Function

When you enable auto-negotiation on the 1000BASE-X PCS function and link synchronization is acquired, the auto-negotiation process could not complete.

Affected Configuration

This issue affects 1000BASE-X PCS function designs with the auto-negotiation option enabled.

Workaround

Set the HD bit in the dev_ability register to 1.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Warning Messages for Stratix V Designs

When you compile a design that targets a Stratix V device, the Quartus II software displays the following warning messages for various values of *<suffix>*:

Warning: Ignored filter: *alt_xcvr_csr_<suffix> could not be matched with a register

Warning: Ignored set_false_path: Argument <to> is an empty collection

Warning: Ignored filter: *altera_tse_reset_synchronizer_chain*|aclr could not be matched with a pin

You may safely ignore the warning messages.

Affected Configuration

This issue affects all Stratix V designs.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Simulation Fails for Stratix V Designs Instantiated Using SOPC Builder

When you use SOPC Builder to instantiate a design that targets a Stratix V device, the simulation fails for both the VHDL or Verilog HDL files.

Affected Configuration

This issue affects all Stratix V designs instantiated using SOPC Builder.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Unconstraint Clock in Stratix V Designs with GXB Transceiver and Transceiver Reconfiguration Controller Megafunction

When you run a full timing analysis on a Stratix V design that contains a GXB transceiver block and a Transceiver Reconfiguration Controller megafunction, the TimeQuest timing analyzer reports an unconstraint clock. The timing report shows the following:

```
alt_xcvr_arbiter:pif[0].pif_arb|grant[0] was determined to be a clk but was found wt/o an associated clock assignment
```

Affected Configuration

This issue affects Stratix V designs that contain GXB transceiver block and Transceiver Reconfiguration Controller megafunction.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Timing Not Met in Stratix V Devices

Multi-port Triple Speed Ethernet MegaCore function designs that target Stratix V devices may not meet timing requirements.

Affected Configuration

This issue affects multi-port Triple Speed Ethernet MegaCore function designs that target Stratix V devices.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Critical Warning Message for Stratix V Devices

When you compile a design that contains an LVDS SERDES megafunction and targets a Stratix V device, the Quartus II software displays a warning message similar to the following:

```
Critical Warning: DIVCLK port on the PLL is not properly connected on
instance
altera_tse_pcs_pma:altera_tse_pcs_pma_inst|altera_tse_pma_lvds_rx:the_alte
ra_tse_pma_lvds_rx|altlvds_rx:ALTLVDS_RX_component|lvds_rx_ofs3:auto_gener
ated|pll_sclk~PLL_OUTPUT_COUNTER. The output clock port on the PLL must be
connected.
```

Affected Configuration

This issue affects all Stratix V designs that contain LVDS SERDES megafunction.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Critical Warning Messages for 1000BASE-X/SGMII PCS Functions

When you compile designs that contain 1000BASE-X/SGMII PCS function, the Quartus II software displays the following warning messages:

Critical Warning: "mixed_port_feed_through_mode" parameter of RAM atom altera_tse_mac_pcs_pma_gige:altera_tse_mac_pcs_pma_gige_inst|altera_tse_mac_pcs_pma_strx_gx_ena:altera_tse_mac_pcs_pma_strx_gx_ena_inst|altera_tse_top_1000_base_x_strx_gx:top_1000_base_x_strx_gx_inst|altera_tse_top_sgmiis_trx_gx:U_SGMII|altera_tse_top_rx_converter:U_RXCV|altera_tse_a_fifo_24:U_DSW|altera_tse_sdpam_altsyncram:U_RAM|altsyncram:altsyncram_component|altsyncram_q2e1:auto_generated|ram_block1a8 cannot have value "old" when different read and write clocks are used.

Critical Warning: "mixed_port_feed_through_mode" parameter of RAM atom altera_tse_mac_pcs_pma_gige:altera_tse_mac_pcs_pma_gige_inst|altera_tse_mac_pcs_pma_strx_gx_ena:altera_tse_mac_pcs_pma_strx_gx_ena_inst|altera_tse_top_1000_base_x_strx_gx:top_1000_base_x_strx_gx_inst|altera_tse_top_sgmiis_trx_gx:U_SGMII|altera_tse_top_rx_converter:U_RXCV|altera_tse_a_fifo_24:U_DSW|altera_tse_sdpam_altsyncram:U_RAM|altsyncram:altsyncram_component|altsyncram_q2e1:auto_generated|ram_block1a7 cannot have value "old" when different read and write clocks are used.

You may safely ignore the warning messages.

Affected Configuration

This issue affects all designs that contain 1000BASE-X/SGMII PCS function.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Critical Warning Messages When Local Loopback is Enabled

If you enable local loopback on the MAC functions's MII, GMII, or RGMII, the Quartus II software displays the following warning messages when you compile the designs:

Critical Warning: "mixed_port_feed_through_mode" parameter of RAM atom altera_tse_mac:altera_tse_mac_inst|altera_tse_top_gen_host:top_gen_host_inst|altera_tse_top_w_fifo_10_100_1000:U_MAC_TOP|altera_tse_loopback_ff:U_LBFF|altera_tse_a_fifo_24:U_LBFF|altera_tse_sdpam_altsyncram:U_RAM|altsyncram:altsyncram_component|altsyncram_o4e1:auto_generated|ram_block1a8 cannot have value "old" when different read and write clocks are used.

Critical Warning: "mixed_port_feed_through_mode" parameter of RAM atom altera_tse_mac:altera_tse_mac_inst|altera_tse_top_gen_host:top_gen_host_inst|altera_tse_top_w_fifo_10_100_1000:U_MAC_TOP|altera_tse_loopback_ff:U_LBFF|altera_tse_a_fifo_24:U_LBFF|altera_tse_sdpm_altsyncram:U_RAM|altsyncram:altsyncram_component|altsyncram_o4e1:auto_generated|ram_block1a7 cannot have value "old" when different read and write clocks are used.

You may safely ignore the warning messages.

Affected Configuration

This issue affects all designs with local loopback enabled on the MAC's MII, GMII or RGMII.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Critical Warning Message for HardCopy Devices

When you compile a design that contains an LVDS transceiver block and targets a HardCopy device, the Quartus II software displays a warning message similar to the following:

Critical Warning: The following clock transfers have no clock uncertainty assignment. For more accurate results, apply clock uncertainty assignments or use the derive_clock_uncertainty command.

You may safely ignore the warning message. When you verify the timing results in the TimeQuest timing analyzer, you will not see the critical warning in the timing report.

Affected Configuration

This issue affects all HardCopy designs that contain LVDS transceiver blocks.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Fitter Error for Cyclone IV GX Devices with 1000BASE-X/SGMII PCS Functions

In a design that includes a 1000BASE-X/SGMII PCS function and targets a Cyclone IV GX device, the REFCLK used for the 1000BASE-X/SGMII PCS function do not have access to GCLK network. When you compile the design in the Quartus II software, the Fitter module cannot fit the design and reports an error.

Affected Configuration

This issue affects all designs that include 1000BASE-X/SGMII PCS functions and target Cyclone IV GX devices.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Late Collision in Half-Duplex 10/100-Mbps Ethernet MAC

MAC function with 1000BASE-X/SGMII PCS may detect late collision when it is operating in 10/100-Mbps half-duplex mode. The external third party PHY and cables introduce latency in addition to the latency of the 1000BASE-X/SGMII PCS with embedded PMA. This issue arises when the total latency exceeds the 512-bit slotTime as defined in IEEE 802.3 Clause 4.4.

Affected Configuration

This issue affects MAC function designs that contain 10/100/1000-Mbps Ethernet MAC with 1000BASE-X/SGMII PCS operating in 10/100-Mbps half-duplex mode.

Workaround

Use 10/100/1000-Mbps Ethernet MAC only with GMII/MII or RGMII for 10/100-Mbps half-duplex mode operation.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Packet Loss in 8-bit Internal FIFO Buffer

When you enable the SGMII on the MAC function with 8-bit internal FIFO buffer, the MAC function will not transmit the first packet into the FIFO buffer.

Affected Configuration

This issue affects MAC function designs with 8-bit internal FIFO buffer and SGMII PCS.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Speed Change Causes Corrupt Packet

When you switch the MAC speed from 10/100-Mbps to 1000-Mbps while the MAC function is transmitting data, the transmit packet gets corrupted. The MAC function continuously sends data out through the SGMII.

Affected Configuration

This issue affects all designs that contain MAC function with SGMII PCS.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Statistics Counters Issues

Statistics counters are registers that collect statistics on the transmit and receive datapaths in the MAC function. When statistics counters are enabled in any MAC variant, you may observe these issues in various configurations:

- `ifOutUcastPkts` and `ifOutBroadcastPkts` do not increase when the MAC function transmits erroneous unicast and broadcast frames.
- `aFramesReceivedOK` does not increase when the MAC function in 10/100-Mbps variation receives a pause frame.
- `ifInBroadcastPkts` increases when the MAC function in 1000-Mbps variation receives a pause frame.
- `aOctetsReceivedOK` and `etherStatsUndersizePkts` do not count the length of pause frame when you disable the pause frame forwarding on receive.
- `ifOutErrors`, `ifOutUcastPkts`, `ifOutMulticastPkts` and `ifOutBroadcastPkts` do not count the flushed packets when late collision or excessive collision occurs.
- `aFramesReceivedOK`, `aOctetsReceivedOK`, `etherStatsOctets`, `etherStatsPkts` and `etherStatsPkts64Octets` count an extra frame when the MAC function receives a pause frame.
- `aFrameReceivedOK` and `etherStatsUndersizePkts` increase by 1 when the MAC function receives magic packet and wakes up. These statistics counters should not increase in sleep mode.
- All statistics counters operate in normal mode when the MAC function operates in sleep mode.

Affected Configuration

This issue affects variants of MAC with enabled statistics counters.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Continuous Data Transmission from MAC Function

When you switch the MAC function from half-duplex to full-duplex mode while it is transmitting data, the MAC function continuously sends data out through the MII even when you are not sending any data to the MAC function.

Affected Configuration

This issue affects variants of MAC with internal FIFO buffer operating in half-duplex mode.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Half-Duplex Mode Post Collision Issues

When the MAC function operates in half-duplex mode, these issues are observed after collisions:

- The MAC function continuously sends data out through the MII even when you do not send any data to the MAC function.
- No retransmit frame is available on the MAC transmit datapath when collision happens on half-duplex 10Mbps MAC variant.
- The MAC function fails to copy the start of packet (SOP) of the subsequent frame after the retransmit frame into the retransmit buffer.

Affected Configuration

This issue affects variants of MAC function operating in half-duplex mode.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Transceiver Quad Sharing Failure

In designs containing multiple PMA blocks with GXB transceivers, the transceiver channels fail to share one transceiver quad when you instantiate the Triple Speed Ethernet MegaCore functions individually.

Affected Configuration

This issue affects designs that contain all transceiver family devices.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

PLL Sharing Problem for LVDS Channels

In designs containing multiple PMA Blocks with LVDS I/O, the LVDS channels from different Triple Speed Ethernet MegaCore functions fail to share a common PLL.

Affected Configuration

This issue affects designs that contain the Stratix II, Stratix II GX, Stratix III and Stratix IV E/GX device families.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Reset Synchronization Problem

The reset_rx_clk and reset_tx_clk signals do not synchronize to rx_clk and tx_clk.

Affected Configuration

This issue affects variants of MAC function with 1000BASE-X/SGMII PCS and embedded PMA.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

MII Local Loopback Failure

The MAC function receives corrupt data packet when you enable the local loopback on MII.

Affected Configuration

This issue affects designs that contain Triple Speed Ethernet MAC operating at 10/100-Mbps.

Workaround

None.

Solution Status

This issue is fixed in version 11.0 of the Triple Speed Ethernet MegaCore function.

Compilation Targeting a Stratix V Device Fails

Designs that include a Triple Speed Ethernet MegaCore function and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

This issue affects all Triple Speed Ethernet MegaCore function designs that target a Stratix V device.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Simulation Fails for HardCopy IV GX with GXB Transceiver

Simulation fails when you enable the SGMII mode in designs that contain SGMII PCS variations with GXB transceiver and target HardCopy IV GX devices.

Affected Configuration

This issue affects all HardCopy IV GX designs that contain GXB transceiver blocks.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Corrupted Packets in 10/100-Mbps Designs with GXB Transceiver

The rate match FIFO in the transceiver compensates for the frequency difference between the recovered clock and the receive clock by inserting or removing inter-packet gaps between packets. You may observe corrupted packets in variations of the MegaCore function operating at 10/100 Mbps with GXB transceiver for certain combinations of ppm difference and packet size. For 200 ppm difference, the largest supported ppm difference, you get corrupted packets if the packet size is greater than 160 bytes in 10-Mbps designs or 1600 bytes in 100-Mbps designs.

Affected Configuration

This issue affects all designs that contain SGMII PCS variations with GXB transceiver operating at 10/100 Mbps.

Workaround

Set the GXB transceiver to operate in basic mode. To do so, you must instantiate the MegaCore function with an external transceiver. The [Instantiate TSE with External ALTGX / ALTIVDS](#) page includes a design example that demonstrates this configuration and lists the required parameter settings.

Solution Status

This issue is fixed in version 10.1 of the Triple Speed Ethernet MegaCore function.

Serial Loopback is Enabled by Default in Cyclone IV GX Devices

The serial loopback option in designs that target Cyclone IV GX devices is always turned on by default, which is different from designs targeting other device families.

Affected Configuration

This issue affects all Cyclone IV GX designs that contain GXB transceiver blocks.

Workaround

Using the MegaWizard Plug-in Manager, edit the transceiver variation file for Cyclone IV GX, `<project directory>/triple_speed_ethernet-library/altera_tse_altgx_civgx_gige.v`. In the transceiver MegaWizard Interface, turn off the serial loopback option and click **Finish** to regenerate the transceiver variation.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Unstable Designs with LVDS in Hardware

You may get unstable results when running designs that contain LVDS transceiver blocks in hardware. This is caused by the constraints provided with the MegaCore function.

Affected Configuration

This issue affects all configurations that contain LVDS transceiver blocks.

Workaround

Edit the constraint file, *<project directory>/<variation name>_constraint.sdc*, and replace lines 410 through 417 with the following lines:

```
set_clock_groups -asynchronous \  
-group {altera_tse_mac_rx_clk_0} \  
-group {altera_tse_mac_tx_clk_0} \  
-group {altera_tse_rx_afull_clk} \  
-group {altera_tse_sys_clk} \  
-group {altera_tse_ref_clk} \  
altera_tse_multi_mac_pcs_pma_inst|the_altera_tse_pma_lvds_rx_0|altlvds_  
rx_component|auto_generated|rx[0]|clk0 \  
altera_tse_multi_mac_pcs_pma_inst|the_altera_tse_pma_lvds_rx_0|altlvds_  
rx_component|auto_generated|pll|clk[0]}
```

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Timing Not Met in Cyclone III Devices

Designs targeted to Cyclone III devices may not meet timing when the skew optimization option is turned on by default.

Affected Configuration

This issue may affect variations in designs targeted to Cyclone III devices.

Workaround

Turn off the skew optimization option by adding the following assignment in the Quartus II settings file (*.qsf*):

```
set_global_assignment -name ENABLE_BENEFICIAL_SKEW OPTIMIZATION OFF
```

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of Bit `PAGE_RECEIVE` in PCS Register

The Triple Speed Ethernet MegaCore function sets the `PAGE_RECEIVE` bit in the PCS register `an_expansion` to 1 when a /C/ ordered set is received. This behavior does not comply with the IEEE 802.3 Standard clause 37.

Affected Configuration

This issue affects all configurations that include the PCS function.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of `aAlignmentError` Statistics Counter

The Triple Speed Ethernet MegaCore function increments the `aAlignmentError` statistics counter when an SFD error is encountered. This behavior does not comply with the IEEE 802.3 Standard clause 5.2.2.1.7.

Affected Configuration

This issue affects all configurations.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Revision History

Table 33–1 shows the revision history of the Video and Image Processing Suite MegaCore functions.



For information about the new features, refer to the *Video and Image Processing Suite User Guide*.

Table 33–1. Video and Image Processing Suite Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Added Deinterlacer II MegaCore function. Added new polyphase calculation method for Scaler II MegaCore function. Final support for Arria II GX, Arria II GZ, and Stratix V devices.
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	<ul style="list-style-type: none"> Added Scaler II MegaCore function. Final support for Stratix IV GT devices.
10.0	July 2010	<ul style="list-style-type: none"> Added Interlacer MegaCore function. Updated Clocked Video Output and Clocked Video Input MegaCore functions to insert and extract ancillary packets.

Errata

Table 33–2 shows the issues that affect the Video and Image Processing Suite MegaCore functions v11.0, 10.1, and 10.0.



Not all issues affect all versions of the Video and Image Processing Suite MegaCore functions.

Table 33–2. Video and Image Processing Suite Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
1 Jul 11	Video and Image Processing Suite Fails to Launch in Windows			
15 May 11	High Number of Critical Warnings During Compilation for Deinterlacer II and Video Frame Buffer	✓	—	—
	Scaler II Coefficients MIF for Simulation Missing in Qsys	✓	—	—
	Scaler II Generates Incorrect Output When It Receives Elongated Control Packet	Fixed	✓	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—
15 Mar 11	Signed Vertical Coefficients and Unsigned Horizontal Coefficients (or Vice Versa) with Sum of Coefficients More Than 1 Cause Scaler II to Generate Incorrect Output	✓	✓	—
	Scaler II Generates Incorrect Output When Vertical Filter Taps is 3	✓	✓	—

Table 33–2. Video and Image Processing Suite Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 Dec 10	Scaler II Generates Incorrect Output When Receiving Empty Packets	✓	✓	—
	Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly	✓	✓	✓
	Compilation Fails on the Windows 7 or Vista Operating System	✓	✓	✓
15 Feb 10	Compilation Errors with the Frame Buffer	✓	✓	✓
15 Nov 09	Frame Buffer and Deinterlacer are Missing Entry in .sdc File	✓	✓	✓
	Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)	✓	✓	✓
	Scaler: Number of Colour Planes Incorrect	✓	✓	✓
15 Mar 09	RTL Simulation Reports Errors When Using Verilog HDL	✓	✓	✓
	Incorrect Simulation Models Created for Deinterlacer and Frame Buffer	✓	✓	✓
	Deinterlacer and Test Pattern Generator May Not Upgrade	✓	✓	✓
	The 2D Median Filter Does Not Support 7×7 Filter Size	✓	✓	✓
	Packets Sent to VIP Cores Must Have Non-Empty Payload	✓	✓	✓
15 May 08	SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video	✓	✓	✓
01 Oct 07	Scalar Coefficients Preview Window Cannot be Closed	✓	✓	✓
01 May 07	Precision Must be Set When Using Lanczos Coefficients in Scaler	✓	✓	✓
01 Dec 06	Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector	✓	✓	✓

Video and Image Processing Suite Fails to Launch in Windows

Some IP cores in the Video and Image Processing Suite version 11.0 fail to launch in Windows if the installation path for the Windows-platform ACDS contains spaces.

Affected Configurations

This issue affects all the following Video and Image Processing cores installed in Windows platform with spaces in the installation path:

- 2D FIR Filter IP core
- 2D Median Filter IP core
- Chroma Resampler IP core
- Clipper IP core
- Color Plan Sequencer IP core
- Color Space Converter (CSC) IP core
- Clipper IP core
- Deinterlacer IP core
- Frame Buffer IP core
- Gamma Corrector IP core
- Interlacer IP core
- Scaler IP core

- Test Pattern Generator IP core

Design Impact

You cannot access the Video and Image Processing Suite parameters through the MegaWizard Plug-In Manager.

Workaround

Install the ACDS Suite in a directory that does not contain spaces in its path.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

High Number of Critical Warnings During Compilation for Deinterlacer II and Video Frame Buffer

The Quartus II software shows a high number of critical warnings when you compile your designs using the Deinterlacer II or Video Frame Buffer MegaCore function. The critical warnings mainly include the following line:

```
...cannot have value "old" when different read and write clocks are used
```

Affected Configurations

This issue affects all configurations using the Deinterlacer II or Video Frame Buffer MegaCore function version 11.0.

Design Impact

The design gets a high number of critical warnings during compilation.

Workaround

None. It is safe to ignore these critical warnings.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler II Coefficients MIF for Simulation Missing in Qsys

If you instantiate the Scaler II in Qsys and enable create simulation model in either Verilog HDL or VHDL language, the Quartus II software does not generate the coefficients MIF for simulation model in the **simulation/submodules/** folder.

Affected Configurations

This issue affects all configurations that use the Scaler II simulation model with **Bicubic** or **Polyphase** scaling algorithm and **Load scaler coefficients at run time** turned off.

Design Impact

The design fails to simulate and shows the following error:

```
Failed to open <language> file
"<variation_name>_<component_name>_scaler_core_coeff.mif" in r mode and
no such file or directory
```

Workaround

Copy and paste the MIF generated in the **synthesis/submodules** folder to the **simulation/submodules** folder.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler II Generates Incorrect Output When It Receives Elongated Control Packet

The Scaler II MegaCore function with the **Enable run-time control of input/output frame size** option turned on may generate incorrect output when it receives an elongated control packet.

Affected Configurations

This issue affects your system if you instantiate the Scaler II Megacore function directly after you instantiate the Color Plane Sequencer or Chroma Resampler Megacore function.

Design Impact

The affected configuration may generate incorrect output or crash.

Workaround

None. Avoid using the Scaler II MegaCore function with the **Enable run-time control of input/output frame size** option turned on directly after the Color Plane Sequencer or Chroma Resampler Megacore function.

Solution Status

This issue is fixed in version 11.0 of the Video and Image Processing Suite.

Compilation Targeting a Stratix V Device Fails

Designs that include at least one of several IP cores from the Video and Image Processing Suite and target a Stratix V device, do not compile even if you have a valid license for the suite. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

This issue affects designs that target a Stratix V device and include at least one of the following IP cores from the Video and Image Processing Suite:

- 2D FIR Filter IP core
- 2D Median Filter IP core

- Alpha Blending Mixer IP core
- Chroma Resampler IP core
- Clipper IP core
- Color Plan Sequencer IP core
- Color Space Converter (CSC) IP core
- Deinterlacer IP core
- Frame Buffer IP core
- Gamma Corrector IP core
- Interlacer IP core
- Scaler IP core
- Test Pattern Generator IP core

Design Impact

Designs that include at least one of these IP cores and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for the video and image processing IP cores, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Signed Vertical Coefficients and Unsigned Horizontal Coefficients (or Vice Versa) with Sum of Coefficients More Than 1 Cause Scaler II to Generate Incorrect Output

The Scaler II MegaCore function may generate incorrect output when you use signed vertical coefficients with unsigned horizontal coefficients (or vice versa) and the sum of the coefficients for one or more phases is more than 1.

Affected Configurations

This issue affects all configurations that use the polyphase and bicubic algorithms with the Scaler II MegaCore function.

Design Impact

The affected configuration may generate incorrect output.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler II Generates Incorrect Output When Vertical Filter Taps is 3

The Scaler II MegaCore function using polyphase algorithm may generate incorrect output when you set **Vertical Filter Taps** to 3.

Affected Configurations

This issue affects all configurations that use the polyphase algorithms with the Scaler II MegaCore function.

Design Impact

The affected configuration may generate incorrect output.

Workaround

None. If your design allows, set **Vertical Filter Taps** to 4.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler II Generates Incorrect Output When Receiving Empty Packets

The Scaler II MegaCore function generates incorrect output when it receives empty packets with only the header, start of packet (SOP), and end of packet (EOP) on the same clock cycle.

Affected Configurations

This issue affects all configurations that use the Scaler II MegaCore function.

Design Impact

The empty packets sent will be altered.

Workaround

None. You cannot deliberately send empty user packets through the Scaler II MegaCore function expecting unaltered outputs.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly

The Deinterlacer and Frame Buffer MegaCore functions may not work properly when connected to a DDR3 SDRAM High Performance Controller MegaCore function.

In some configurations and or with specific input resolutions, the Deinterlacer and Frame Buffer MegaCore functions may issue write and read bursts starting at odd addresses. The DDR3 SDRAM controller uses wrapping bursts for read accesses, consequently the wrong data may be read back from memory.

Affected Configurations

Systems connecting the Video and Image Processing MegaCore functions to DDR3 SDRAM.

Design Impact

This issue may have unpredictable effects. Typically, the output video is distorted.

Workaround

Turn on **Align read/write bursts with burst boundaries** in the Frame Buffer and Deinterlacer parameter editors.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Compilation Fails on the Windows 7 or Vista Operating System

On the Windows 7 or Vista Operating System, when synthesizing the VIP Suite IP MegaCore functions in the Quartus II software, or generating an IP functional simulation model, compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

For synthesis, you receive the following error:

```
Error: Node instance "scaler" instantiates undefined entity
"alt_vip_scl_GNRA6GTEAK" File: C:/work/testvip/db/scaler_GN.vhd Line:
52
```

For IP functional simulation model generation, you receive the following error:

```
Error: Simulation model map command failed:
D:\altera\90sp2\quartus\bin\quartus_map scaler --simgen --
simgen_parameter="CBX_HDL_LANGUAGE=VHDL"
```

Workaround

You must run the Quartus II software as administrator to enable the VIP Suite IP generation and synthesis to complete successfully. To run Quartus II as administrator on the **Start menu**, point to **Programs**, then **Altera**, then right click on **Quartus II <version>**. Click **Run as administrator**.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Compilation Errors with the Frame Buffer

The frame buffer may fail to generate and issues a compilation error when you turn on **Discard invalid frames/fields**.

Affected Configurations

This issue affects configurations that use the **Discard invalid frames/fields** option without turning on either the frame dropping or the support for interlaced fields.

Design Impact

The generation fails and you receive the following compilation errors:

```
Error: IP Generator Error: At end of source: error: expected a "}"  
Error: IP Generator Error:  
"C:/altera/91/ip/altera/frame_buffer/lib/vip_vfb_hwfast.hpp", line  
756: error: expected "while"
```

Workaround

This issue has no workaround. However, enabling the support for interlaced video may be an acceptable solution for video systems where the frame buffer is only processing progressive frames.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Frame Buffer and Deinterlacer are Missing Entry in .sdc File

You must manually add the Synopsis Design Constraint (**.sdc**) files to the Quartus II project for the following MegaCore functions:

- Deinterlacer
- Frame Buffer
- Clocked Video Input
- Clocked Video Output

Affected Configurations

All configurations that use any of these MegaCore functions.

Design Impact

These **.sdc** files declare false paths that the Quartus II software should not consider during timing analysis. Timing closure for valid critical paths may not be achievable if you do not include these files in your project, which results in a nonfunctioning system.

Workaround

Add the .sdc files manually from the project settings windows. In the Quartus II software, on the Project menu click **Add/Remove Files in Project**. Altera provides these .sdc files with your Quartus II installation and are in the following directory:

```
<install_dir>\ip\<megacore_function>\lib\alt_vip_<tla>.sdc
```

where:

- <megacore_function> is **deinterlacer**, **frame_buffer**, **clocked_video_input**, or **clocked_video_output**
- <tla> is an acronym that identifies the MegaCore function

To verify that the Quartus II software correctly adds the .sdc files, keep the **Settings** window open and click **Timing Analysis Settings** then **TimeQuest Timing Analyzer** in the tree menu.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)

When you turn on frame locking in the **Clocked Video Output** it attempts to align its start of frame (output by the vid_sof signal) to the incoming start of frame signal (the sof signal). When it achieves this alignment, the IP core frame locks the output video (the start of frames are aligned) to the input video.

Affected Configurations

This issue affects systems enabling the frame locking functionality in the **Clocked Video Output**.

Design Impact

The output video frame lock is out by one cycle.

Workaround

To work around this issue, move the **Clocked Video Output** start of frame one cycle earlier. For example, if the start of frame required for **Mode 1** is at sample 10, write 9 into bits 2 to 15 of the Model SOF Sample register.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler: Number of Colour Planes Incorrect

The **Scaler: Number of colour planes** should be 1 to 3.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

RTL Simulation Reports Errors When Using Verilog HDL

EDA RTL simulation started from the Quartus II software reports errors in the ModelSim® simulator for designs containing Video and Image Processing Suite MegaCore functions when the output files are in Verilog HDL.

Affected Configurations

This issue affects configurations that use NativeLink to run a ModelSim simulation from Verilog HDL.

Design Impact

An error message reports that software cannot find the Altera library.

Workaround

Compile the file `db/alt_cusp90_package.vhd` to the Altera library. To perform this compilation, modify the top-level `.do` script in the `simulation/modelsim` directory.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Incorrect Simulation Models Created for Deinterlacer and Frame Buffer

The Quartus II software may create incorrect functional simulation models for the Deinterlacer and Frame Buffer MegaCore functions.

Affected Configurations

This issue affects configurations that use a different clock domain for the Avalon Memory-Mapped (Avalon-MM) master interfaces.

Design Impact

The IP functional simulation models generated with the MegaWizard Plug-in may reset in an incorrect state. This issue may also affect simulation models generated with SOPC Builder.

Workaround

If possible, release the reset signals for the Avalon-MM interface ports before the reset signal for the MegaCore function. Alternatively, repeat the generation until the wizard produces a valid `.vo` or `.vho` file.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Deinterlacer and Test Pattern Generator May Not Upgrade

The Deinterlacer and Test Pattern Generator MegaCore functions may not directly upgrade to v9.0 in SOPC Builder.

Affected Configurations

This issue affects the Quartus II v8.1 designs containing Deinterlacer or Test Pattern Generator MegaCore functions that were originally created in the Quartus II v8.0 software.

Design Impact

SOPC Builder reports an error when it tries to upgrade the MegaCore function if you do not change the parameterization.

Workaround

To workaroud this issue, follow these steps:

1. Open the v8.1 version of your design.
2. Make a change to the parameterization of any Deinterlacer or Test Pattern Generator MegaCore functions and apply your change.
3. Change back to the original parameterization, then save the SOPC Builder system.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

The 2D Median Filter Does Not Support 7×7 Filter Size

The 2D Median Filter MegaCore function does not support the 7×7 filter size.

Affected Configurations

This issue affects configurations that include the 2D Median Filter MegaCore function.

Design Impact

You can select a 7×7 filter size in pre-9.0 versions of the 2D Median Filter MegaCore function but the software issues an error message when generating the simulation model.

Workaround

There is no workaround. Do not select the 7×7 filter size.

Solution Status

The 7×7 filter size is not available in version 9.0 or later of the Video and Image Processing Suite.

Packets Sent to VIP Cores Must Have Non-Empty Payload

The packets sent to the Color Space Converter and 2D Median Filter MegaCore functions must have non-empty payload. If a packet is sent with a type but without any further information, the packet processing logic may enter an inconsistent state.

Affected Configurations

This issue affects configurations that include the Color Space Converter or 2D Median Filter MegaCore functions.

Design Impact

If the IP core receives a packet with an empty payload, it may not output correct data until it receives a few non-empty packets.

Workaround

If you intend to send an empty packet, send one symbol of data with it.

Solution Status

This issue is unlikely to be fixed as there is a simple workaround.

SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video

In SOPC Builder, the Avalon-ST data adapter does not support the Avalon-ST Video protocol. No error message is currently displayed when connecting the components.

Affected Configurations

This issue affects SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function.

Design Impact

Connecting any of the Video and Image Processing Suite MegaCore functions to an Avalon-ST data adapter results in a generated system in which the Avalon-ST video protocol is corrupted.

Workaround

To connect Video and Image Processing MegaCore functions that have a different number of planes in parallel, use the Color Plane Sequencer. For example: to convert between 3 colors in parallel (3 symbols per beat) and 3 colors in sequence (1 symbol per beat).

Solution Status

You cannot connect unsupported Avalon-ST adapters in a future version of SOPC Builder and the Video and Image Processing Suite.

Scalar Coefficients Preview Window Cannot be Closed

You cannot close the Scalar Coefficients Preview window when you use it in SOPC Builder.

Affected Configurations

This issue affects the Scaler MegaCore Function when you use the SOPC Builder flow.

Design Impact

This issue does not prevent you from parameterizing the Scalar and therefore has no design impact.

Workaround

The Coefficient Preview window closes when you close the main Scalar parameterization interface.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Precision Must be Set When Using Lanczos Coefficients in Scaler

When configuring the Scaler MegaCore function, you must choose the correct coefficient precision when using Lanczos coefficients.

Affected Configurations

This issue affects configurations of the Scaler MegaCore function using the polyphase algorithm with Lanczos coefficients.

Design Impact

The MegaCore function fails to generate.

Workaround

If you select polyphase mode with Lanczos coefficients, you must set the coefficient precision to be signed with one integer bit. Fraction bits can be set within the full range available in the MegaWizard interface.

Solution Status

The coefficient precision restriction will be enforced in future versions of the Video and Image Processing Suite.

Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector

M4K block write operations may fail for Cyclone II devices with the Alpha Blending Mixer and Gamma Corrector MegaCore functions.

Affected Configurations

This issue affects configurations using Cyclone II devices and the Alpha Blending Mixer or Gamma Corrector MegaCore function.

Design Impact

The Quartus II software issues the following error message:

```
Error: M4K memory block WYSIWYG primitive
"vhdl_gam:vhdl_gam_inst|TTA_X_smem_av:gamma_lut|altsyncram:\dsl:altsyn
cram_component|altsyncram_rvh1:auto_generated|ram_block1a0" utilizes
the dual-port dual-clock mode. However, this mode is not supported in
Cyclone II device family in this version of Quartus II software. Please
refer to the Cyclone II FPGA Family Errata Sheet for more information
on this feature.
```

Workaround

If you target any affected revision (Rev a or b of the 2c35 or Rev a of any other Cyclone II part), set the CYCLONEII_SAFE_WRITE variable to RESTRUCTURE. This setting causes the Quartus II software to fix the issue at a cost in M4Ks and F_{\max} . If you are using a newer revision device, set the CYCLONEII_SAFE_WRITE variable to VERIFIED_SAFE, which turns off the error message.

Solution Status

This issue is fixed for the latest silicon devices but remains an issue if you are using the earlier silicon.



Refer to the [Cyclone II FPGA Family Errata Sheet](#) for more information about this issue.

Revision History

Table 34–1 shows the revision history for the Viterbi Compiler.


 For more information about the new features, refer to the *Viterbi Compiler User Guide*.

Table 34–1. Viterbi Compiler Revision History

Version	Date	Description
11.0	May 2011	<ul style="list-style-type: none"> Final support for Arria II GX, Arria II GZ, Cyclone III LS, and Cyclone IV GX devices. HardCopy Compilation support for HardCopy III, HardCopy IV E, and HardCopy IV GX devices.
10.1	December 2010	<ul style="list-style-type: none"> Preliminary support for Arria II GZ devices. Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.

Errata

Table 34–2 shows the issues that affect the Viterbi Compiler v11.0, v10.1, and v10.0.

 Not all issues affect all versions of the Viterbi Compiler.

Table 34–2. Viterbi Compiler Errata

Added or Updated	Issue	Affected Version		
		11.0	10.1	10.0
15 May 11	Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices	✓	—	—
	Compilation Targeting a Stratix V Device Fails	Fixed	✓	—
15 Mar 09	Testbench ber_clear Signal is Not Connected	✓	✓	✓
	Gate-Level Simulation Fails	✓	✓	✓

Warning Message Indicates Preliminary Support for Arria II GZ and Cyclone IV GX Devices

The Viterbi Compiler v11.0 provides final support for Arria II GZ and Cyclone IV GX devices. However, when your Viterbi Compiler targets an Arria II GZ device or a Cyclone IV GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All Viterbi Compiler variations that target an Arria II GZ device or a Cyclone IV GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

Compilation Targeting a Stratix V Device Fails

Designs that include a Viterbi Compiler and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

Viterbi Compiler designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue is fixed in version 11.0 of the Quartus II software.

Testbench ber_clear Signal is Not Connected

The ber_clear signal in the generated testbench is not connected correctly.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

Gate-Level Simulation Fails

The Viterbi Compiler does not support gate-level simulations.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

Revision History

Table 35–1 shows the revision history for the XAUI PHY IP core.



For more information about the new features, refer to the “XAUI PHY IP Core” chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 35–1. XAUI PHY Revision History

Version	Date	Description
11.0	May 2011	Added support for DXAUI. Added support for Arria II GZ and HardCopy IV.
10.1	December 2010	Added support for Arria II GX and Cyclone IV GX with hard PCS.
10.0 SP1	September 2010	Added simulation support.
10.0	July 2010	First release.

Errata

Table 35–2 shows the issues that affect the XAUI PHY IP core versions 11.0, 10.1, 10.0 SP1, and 10.0.

Table 35–2. XAUI PHY Errata

Added or Updated	Issue	Affected Version			
		11.0	10.1	10.0 SP1	10.0
15 Dec 10	Mixed Language Simulation Fails when Optimization Is On	✓	✓	—	—
15 Sept 10	TimeQuest Timing Analyzer Might Improperly Report Setup Violations	—	—	Fixed	✓
15 Aug 10	Incorrect Addresses for XAUI Reset, RX and TX Control and Status Registers	—	Fixed	✓	✓

Mixed Language Simulation Fails when Optimization Is On

Simulation fails when using ModelSim with mixed-languages.

Affected Configurations

This issue affects mixed language simulation including Verilog modules and VHDL entities when optimization is on.

Workaround

The workaround is to turn ModelSim optimization off by using the `-novpt` option to the `vsim` command.

Solution Status

This issue may be fixed in a future version of ModelSim.

TimeQuest Timing Analyzer Might Improperly Report Setup Violations

During timing analysis of a soft XAUI PHY MegaCore function, the TimeQuest Timing Analyzer might report setup violations within the `mgmt_clk_clk` domain and between the `mgmt_clk_clk` and another clock domain. The TimeQuest Timing Analyzer might also report hold time violations.

Affected Configurations

This issue affects the soft IP implementation of the XAUI PHY IP core in Stratix V devices.

Workaround

The majority of paths that show violations are between asynchronous signals and consequently are false timing paths. In addition, because there is no relationship between the `mgmt_clk_clk` and `refclk_clk`, these timing violations represent false paths. To eliminate timing errors for these false paths, you can add the statements in [Example 35-1](#) to your Synopsis Design Constraints File (`.sdc`).

Example 35-1. False Timing Paths for the `mgmt_clk_clk` Clock Domain

```
set_false_path -from [get_clocks refclk_clk] -to [get_clocks mgmt_clk_clk]
set_false_path -from [get_clocks mgmt_clk_clk] -to [get_clocks refclk_clk]
set_false_path -from [get_clocks
{*|alt_pma_0|alt_pma_sv_inst|sv_xcvr_generic_inst|channel_tx[0].duplex_pcs|ch[0].rx_pcs|clocktopld}] -to [get_clocks mgmt_clk_clk]
```

The timing paths in the `mgmt_clk_clk` domain shown in [Example 35-2](#) are not false paths; however, you can ignore these errors or other errors that are within the soft XAUI IP core.

Example 35-2. Timing Violations for the `mgmt_clk_clk` Clock Domain

```
1. From Node
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|chnl_ad
dr_reg[7]
; To Node
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|analog_
reconfig_readdata[2] ;

2. From Node
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|chnl_ad
dr_reg[7]
; To Node
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|analog_
reconfig_readdata[3] ;
```

Finally, the soft IP implementation of the XAUI PHY might show hold time violations which may also be safely ignored.

No workaround is required.

Solution Status

This issue is fixed in release 10.0 SP1 of the soft XAUI PHY IP core.

Incorrect Addresses for XAUI Reset, RX and TX Control and Status Registers

The *XAUI IP Core* chapter of the *Altera Transceiver PHY IP Core User Guide* provides incorrect addresses for the XAUI reset, RX and TX control and status registers.

Affected Configurations

This is a documentation issue only. [Table 35–1](#) gives the correct addresses.

Table 35–3. Reset, RX, TX Status and Simulation Registers (Part 1 of 2)

Addr: 0x200

Offset	Register	Field	Description
0x004	RESET	RX_DIGITAL	Resets the Rx PCS clock domain.
		TX_DIGITAL	Resets the Tx PCS clock domain.
0x008	RX_CNTRL	INVPOLARITY[3:0]	Inverts the polarity of corresponding bit. This register is RW.
0x00C	TX_CNTRL	INVPOLARITY[3:0]	Inverts the polarity of corresponding bit. This register is RW.
0x010	RX_STATUS_0	PATTERNDETECT[7:0]	When asserted, indicates that the programmed word alignment pattern has been detected in the current word boundary. The Rx pattern detect signal is 2 bits wide per channel or 8 bits per XAUI link. Reading the value of the pattern detect registers clears the bits.
		SYNCSTATUS[7:0]	Records the synchronization status of the corresponding bit. There are 2 bits per channel for a total of 8 bits per XAUI link.
0x014	RX_STATUS_1	ERRDETECT[7:0]	When set, indicates that a received 10-bit code group has an 8B/10B code violation or disparity error. It is used along with Rx disparity to differentiate between a code violation error and a disparity error, or both. There are 2 bits per channel for a total of 8 bits per XAUI link. Reading the value of the <code>errdetect</code> register clears the bits.
		DISPERR[7:0]	Indicates that the received 10-bit code or data group has a disparity error. When set, the corresponding <code>errdetect</code> bits are also set. There are 2 bits wide per channel for a total of 8 bits per XAUI link. Reading the value of the <code>errdetect</code> register clears the bits.
0x018	RX_STATUS_2	RLV[3:0]	Indicates a run length violation. Asserted, if the number of continuous 1s and 0s exceeds the number that was set in the run-length option. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RLV register clears the bits.
		PHASE_COMP_FIFO_ERROR[3:0]	Indicates a Rx phase compensation FIFO overflow or underrun condition on the corresponding lane. Reading the value of the <code>PHASE_COMP_FIFO_ERROR</code> register clears the bits.

Table 35-3. Reset, RX, TX Status and Simulation Registers (Part 2 of 2)

Addr: 0x200

Offset	Register	Field	Description
0x01C	RX_STATUS_3	RMFIFODATADELETED[7:0]	When asserted, indicates that the rate match block has deleted an R column. The flag goes high for one clock cycle per deleted R column. There are 2 bits for each lane. Reading the value of the RMFIFODATADELETED register clears the bits.
		RMFIFODATAINSERTED[7:0]	When asserted, indicates that the rate match block inserted a R column. Goes high for one clock cycle per inserted R column. cycle per deleted R column. Reading the value of the RMFIFODATAINSERTED register clears the bits.
0x020	RX_STATUS_4	RMFIFOFULL[3:0]	When asserted, indicates that rate match FIFO block is full (20 words). This bit is asserted as long as the FIFO is full and is asynchronous to the Rx data. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RMFIFOFULL register clears the bits.
		RMFIFOEMPTY[3:0]	When asserted, indicates that the rate match FIFO block is empty (5 words). This bit is asserted as long as the FIFO is empty and is asynchronous to the receiver. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RMFIFOEMPTY register clears the bits.
0x024	TX_STATUS_0	PHASE_COMP_FIFO_ERROR[2:0]	Indicates a Tx phase compensation FIFO overflow or underrun condition on the corresponding lane. Reading the value of the PHASE_COMP_FIFO_ERROR register clears the bits.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 10.1 of the XAUI IP Core chapter of the *Altera Transceiver PHY IP Core User Guide*.

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com








Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, D: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .
<i>italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pof file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
Courier type	<p>Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code>, <code>tdi</code>, and <code>input</code>. The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code>.</p> <p>Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code>.</p> <p>Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).</p>
	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.