10. Interfacing an External Processor to an Altera FPGA

ED51011-1.1

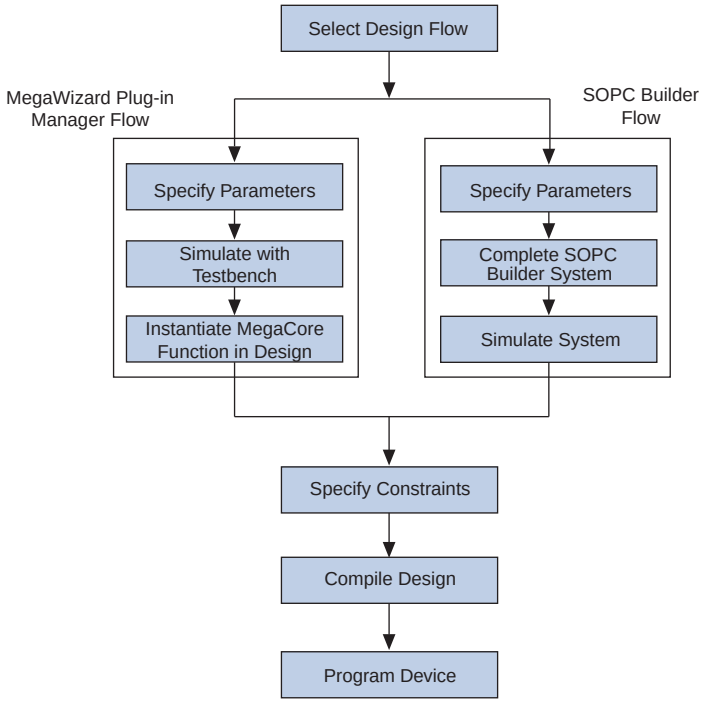
This chapter provides an overview of the options Altera® provides to connect an external processor to an Altera FPGA or Hardcopy® device. These interface options include the PCI Express, PCI, RapidIO®, serial peripheral interface (SPI) interface or a simple custom bridge that you can design yourself.

By including both an FPGA and a commercially available processor in your system, you can partition your design to optimize performance and cost in the following ways:

- Offload pre- or post- processing of data to the external processor
- Create dedicated FPGA resources for co-processing data
- Reduce design time by using IP from Altera's library of components to implement peripheral expansion for industry standard functionality
- Expand the I/O capability of your external processor

You can instantiate the PCI Express, PCI, and RapidIO MegaCore functions using either the MegaWizard™ Plug-In Manager or SOPC Builder design flow. The PCI Lite and SPI cores are only available in the SOPC Builder design flow. SOPC Builder automatically generates the HDL design files that include all of the specified components and system connectivity. Alternatively, you can use the MegaWizard Plug-In Manager to generate a stand-alone component outside of SOPC Builder. Figure 10–1 shows the steps you take to instantiate a component in both design flows.

Figure 10–1. SOPC Builder and MegaWizard Plug-In Manager Design Flows



The remainder of this chapter provides an overview of the MegaCore functions that you can use to interface an Altera FPGA to an external processor. It covers the following topics:

- Configuration Options
- RapidIO Interface
- PCI Express Interface
- PCI Interface
- PCI Lite Interface
- Serial Protocol Interface (SPI)
- Custom Bridge Interfaces

Configuration Options

Figure 10–2 illustrates an SOPC Builder system design that includes a high-performance external bus or switch to connect an industry-standard processor to an external interface of a MegaCore function inside the FPGA. This MegaCore function also includes an Avalon-MM master port that connects to the SOPC Builder system interconnect fabric. As Figure 10–2 illustrates, Altera provides a library of components, typically Avalon-MM slave devices, that connect seamlessly to the Avalon system interconnect fabric.

Figure 10–2. FPGA with a Bus or Switch Interface Bridge for Peripheral Expansion

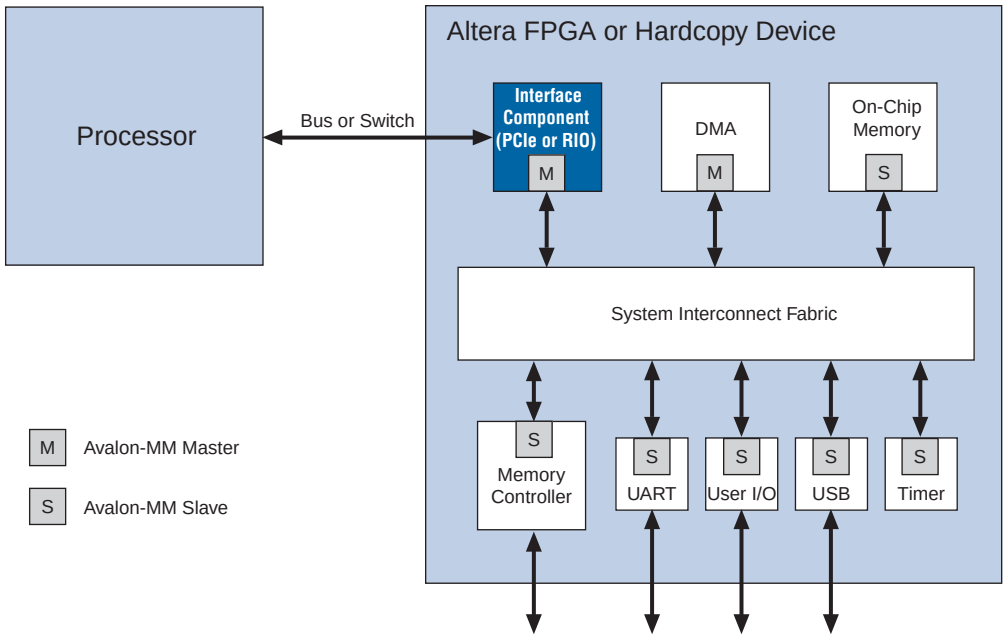
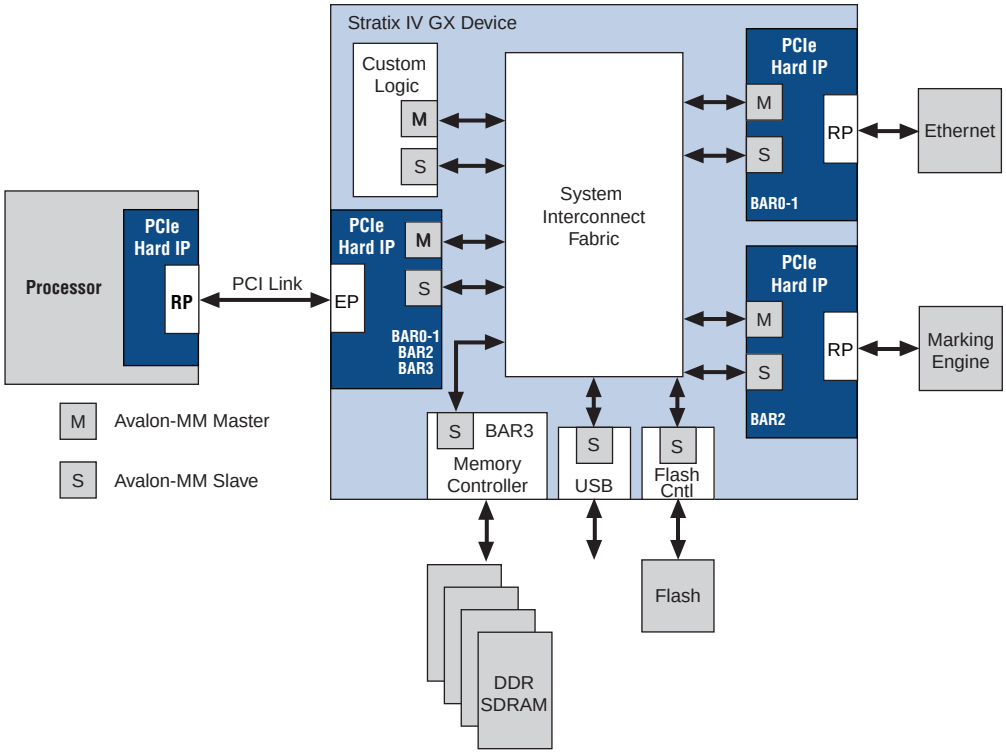


Figure 10–3 illustrates a design that includes an external processor that interfaces to a PCI Express endpoint inside the FPGA. The system interconnect fabric inside the implements a partial crossbar switch between the endpoint that connects to the external processor and two additional PCI Express root ports that interface to an Ethernet card and a marking engine. In addition, the system includes some custom logic, a memory controller to interface to external DDR SDRAM memory, a USB interface port, and an interface to external flash memory. SOPC Builder automatically generates the system interconnect fabric to connect the components in the system.

Figure 10–3. FPGA with a Processor Bus or SPI for Peripheral Expansion



Alternatively, you can also implement your logic in Verilog HDL or VHDL without using SOPC Builder. Figure 10–4 illustrates a modular design that uses the FPGA for co-processing with a second module to implement the interface to the processor. If you choose this option, you must write all of the HDL to connect the modules in your system.

Figure 10–4. FPGA Performs Co-Processing

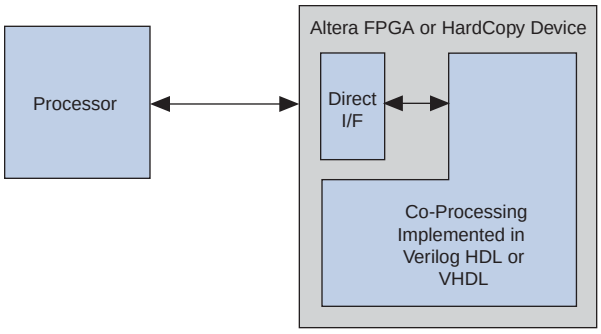


Table 10–1 summarizes the components Altera provides to connect an Altera FPGA or HardCopy device to an external processor. As this table indicates, three of the components are also available for use in the MegaWizard Plug-In Manager design flow in addition to the SOPC Builder. Alternative implementations of these components are also available through the Altera Megafunction Partners Program (AMPP^{SM}) partners. The AMPP partners offer a broad portfolio of megafunctions optimized for Altera devices.

For a complete list of third-party IP for Altera FPGAs, refer to the Intellectual Property & Reference Designs web page of the Altera website. For SOPC Builder components, search for `sopc_builder_ready` in the IP MegaStore megafunction search function.

Table 10–1. Processor Interface Solutions Available from an Altera Device

Protocol	Available in SOPC Builder	Available In MegaWizard Plug-In Manager	Third-Party Solution	OpenCore Plus Evaluation Available
RapidIO	✓	✓	✓	✓
PCI Express	✓	✓	✓	✓
PCI	✓	✓	✓	✓
PCI Lite	✓	—	—	License not required
SPI	✓	—	—	

Table 10–2 summarizes the most popular options for peripheral expansion in SOPC Builder systems that include an industry-standard processor. All of these are available in SOPC Builder. Some are also available using the MegaWizard Plug-In Manager.

Table 10–2. Partial list of peripheral interfaces available for SOPC Builder

Protocol	Available in SOPC Builder	Available In MegaWizard Plug-In Manager	Third-Party Solution	OpenCore Plus Evaluation Available
CAN	✓	—	✓	✓
I2C	✓	—	✓	✓
Ethernet	✓	✓	✓	✓
PIO	✓	—	—	Not required
POS-PHY Level 4 (SPI 4.2)	—	✓	—	✓
SPI	✓	—	✓	Not required
UART	✓	—	✓	✓
USB	✓	—	✓	✓

For detailed information about the components available in SOPC builder refer to the *Embedded Peripherals IP User Guide*.

In some cases, you must download third-party IP solutions from the AMPP vendor website, before you can evaluate the peripheral using the OpenCore Plus.

For more information about the AMPP program and OpenCore Plus refer to *AN343: OpenCore Evaluation of AMPP Megafunctions* and *AN320: OpenCore Plus Evaluation of Megafunctions*.

The following sections discuss the high-performance interfaces that you can use to interface to an external processor.

RapidIO Interface

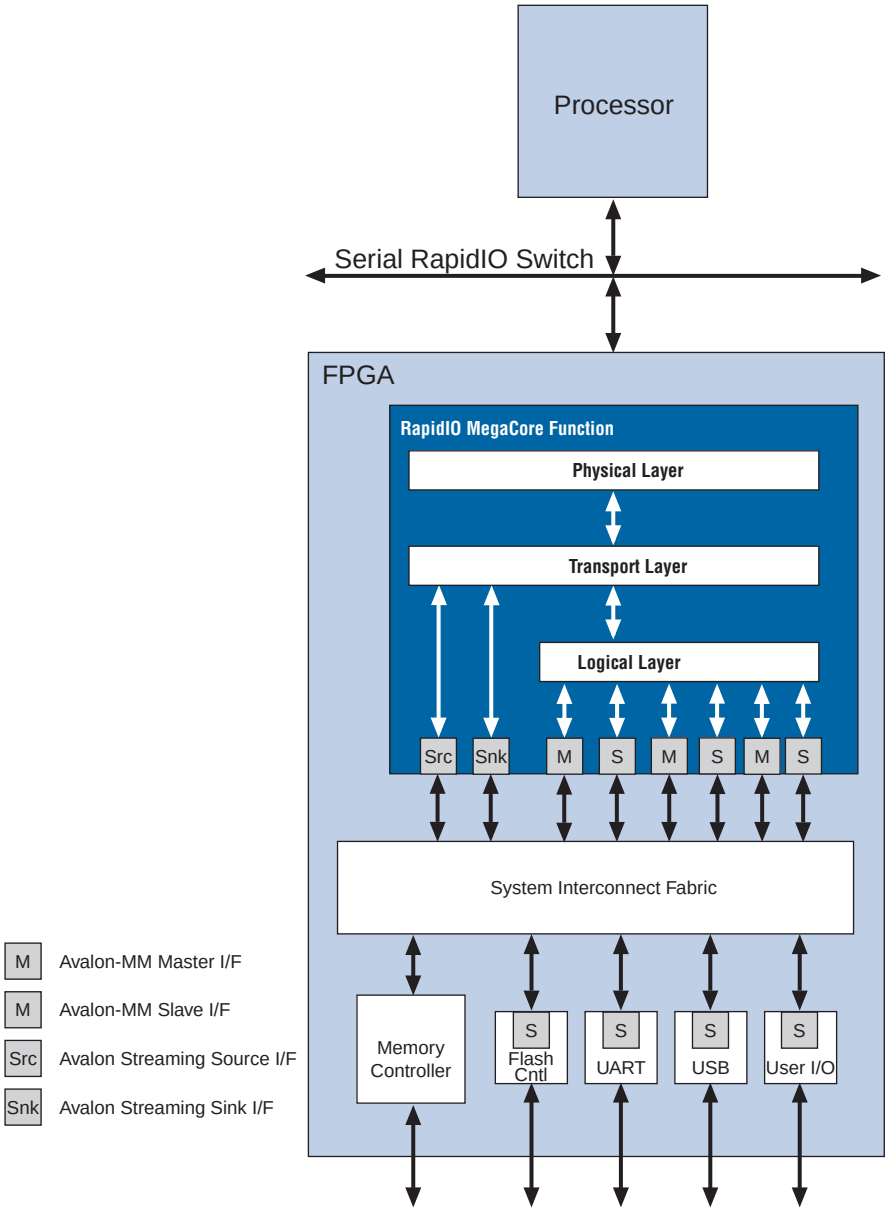
RapidIO is a high-performance packet-switched protocol that transports data and control information between processors, memories, and peripheral devices. The RapidIO MegaCore function is available in SOPC Builder includes Avalon-MM ports that translate Serial RapidIO transactions into Avalon-MM transactions. The MegaCore function also includes an optional Avalon Streaming (Avalon-ST) interface that you can use to send transactions directly from the transport layer to the system interconnect fabric. When you select all optional features, the core includes the following ports:

- Avalon-MM I/O write master
- Avalon-MM I/O read master
- Avalon-MM I/O write slave
- Avalon-MM I/O read slave
- Avalon-MM maintenance master
- Avalon-MM system maintenance slave

- Avalon Streaming sink pass-through TX
- Avalon-ST source pass-through RX

Using the SOPC Builder design flow, you can integrate a RapidIO endpoint in an SOPC Builder system. You connect the ports using the SOPC Builder **System Contents** tab and SOPC Builder automatically generates the system interconnect fabric. Figure 10–5 illustrates an SOPC Builder system that includes a processor and a RapidIO MegaCore function.

Figure 10–5. Example system with RapidIO Interface



Refer to the RapidIO trade association web site's product list at **www.rapidio.org** for a list of processors that support a Rapid IO interface.

Refer to the following documents for a complete description of the RapidIO MegaCore function:

- *RapidIO MegaCore Function User Guide*
- *AN513: RapidIO Interoperability With TI 6482 DSP Reference Design*

PCI Express Interface

The Altera IP Compiler for PCI Express configured using the SOPC Builder design flow uses the IP Compiler for PCI Express's Avalon-MM bridge module to connect the IP Compiler for PCI Express component to the system interconnect fabric. The bridge facilitates the design of PCI Express systems that use the Avalon-MM interface to access SOPC Builder components. Figure 10–6 illustrates a design that links an external processor to an SOPC Builder system using the IP Compiler for PCI Express.

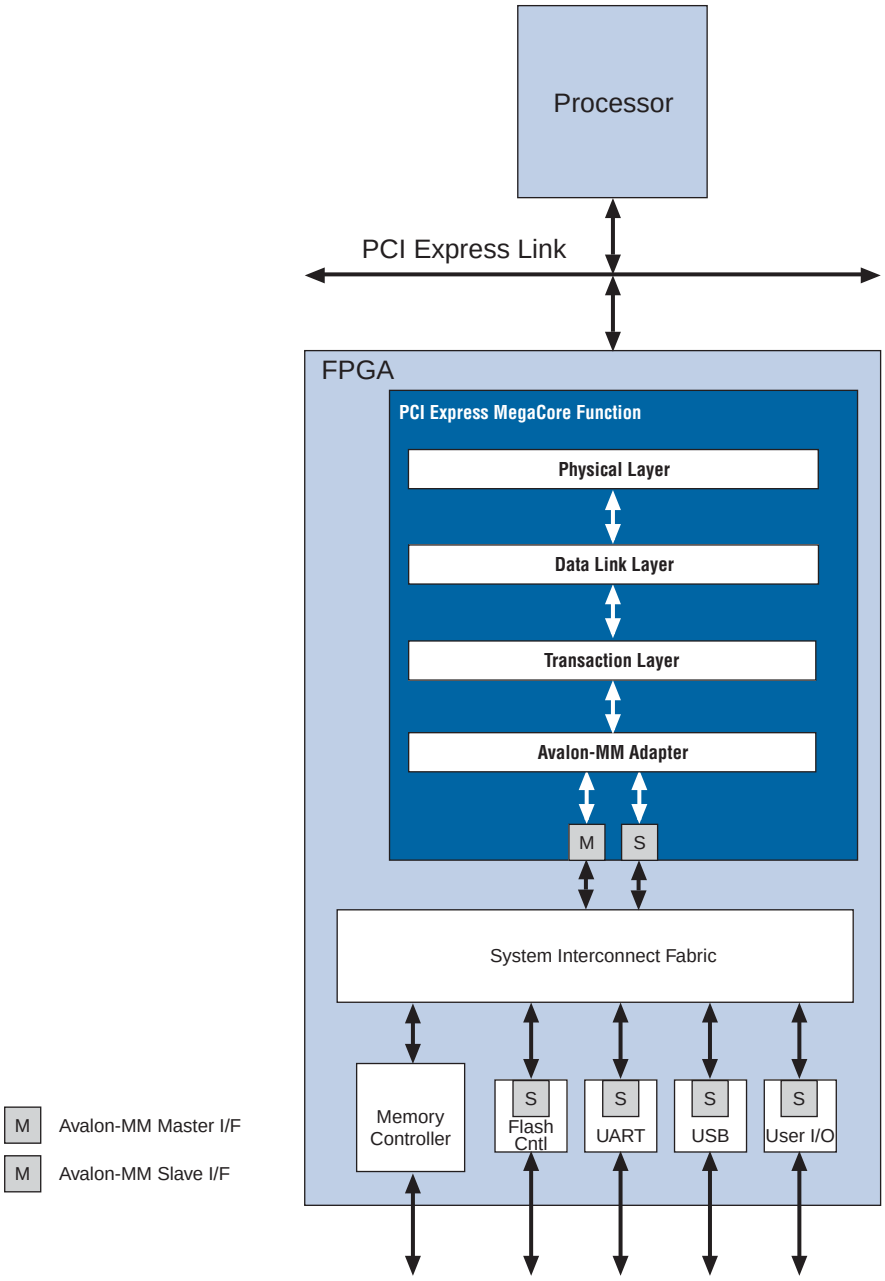
You can also implement the IP Compiler for PCI Express using the MegaWizard Plug-In Manager design flow. The configuration options for the two design flows are different. The IP Compiler for PCI Express is available in Stratix IV and Arria II GX devices as a hard IP implementation and can be used as a root port or end point. In Stratix V devices, Altera provides the Stratix V Hard IP for PCI Express.

For more information about using the IP Compiler for PCI Express refer to the following documents:

- *IP Compiler for PCI Express User Guide*
- *AN532: An SOPC Builder PCI Express Design with GUI Interface*
- *AN456: PCI Express High Performance Reference Design*
- *AN443: External PHY Support in PCI Express MegaCore Functions*
- *AN431: PCI Express to External Memory Reference Design*

Figure 10–6 shows an example system in which an external processor communicates with an Altera FPGA through a PCI Express link.

Figure 10–6. Example system with PCI Express interface

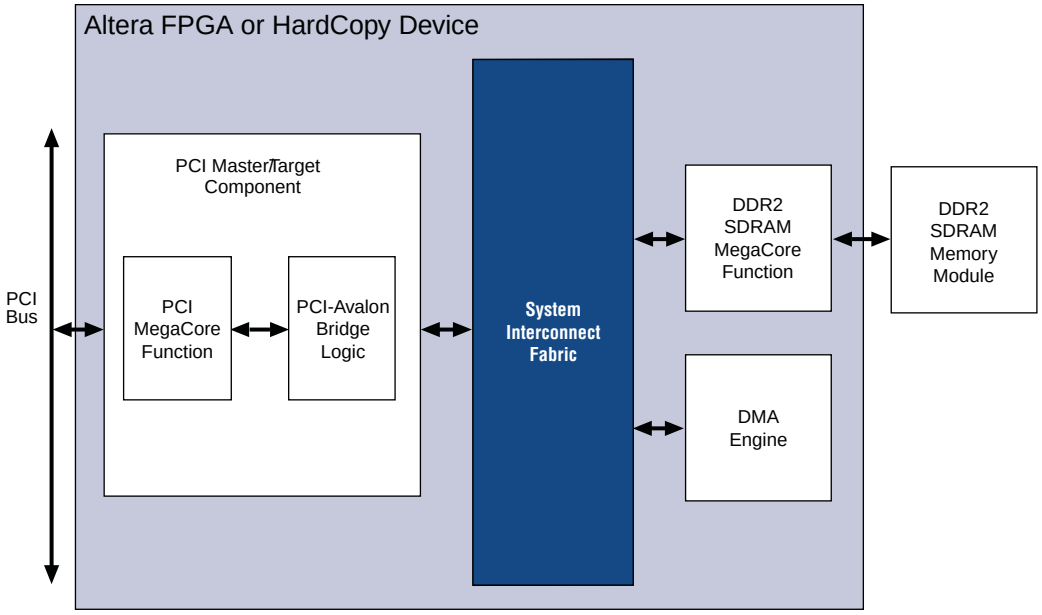


PCI Interface

Altera offers a wide range of PCI local bus solutions that you can use to connect a host processor to an FPGA. You can implement the PCI MegaCore function using the MegaWizard Plug-In Manager or SOPC Builder design flow.

The PCI SOPC Builder flow is an easy way to implement a complete Avalon-MM system which includes peripherals to expand system functionality without having to be well-acquainted with the Avalon-MM protocol. Figure 10–7 illustrates an SOPC Builder system using the PCI MegaCore function. You can parameterize the PCI MegaCore function with a 32- or 64-bit interface.

Figure 10–7. PCI MegaCore Function in an SOPC Builder System



For more information refer to the *PCI Compiler User Guide*.

PCI Lite Interface

The PCI Lite component is optimized for low-latency and high throughput designs. It is available only in the SOPC Builder design flow. The PCI Lite core provides a subset of the PCI MegaCore function feature set to obtain a low-latency path that interfaces to a processor and other peripherals connected to the system interconnect fabric in an FPGA. This component translates PCI transactions to Avalon-MM transactions. The PCI Lite core uses the PCI-Avalon bridge to connect the PCI bus to the system interconnect fabric, allowing you to easily create simple PCI systems that include one or more SOPC Builder components.

For more information refer to the *PCI Lite Core* chapter in the *Embedded Peripherals IP User Guide*.

You can also implement the original PCI master/target and target MegaCore functions without an Avalon-MM bridge module using the MegaWizard Plug-In Manager design flow.

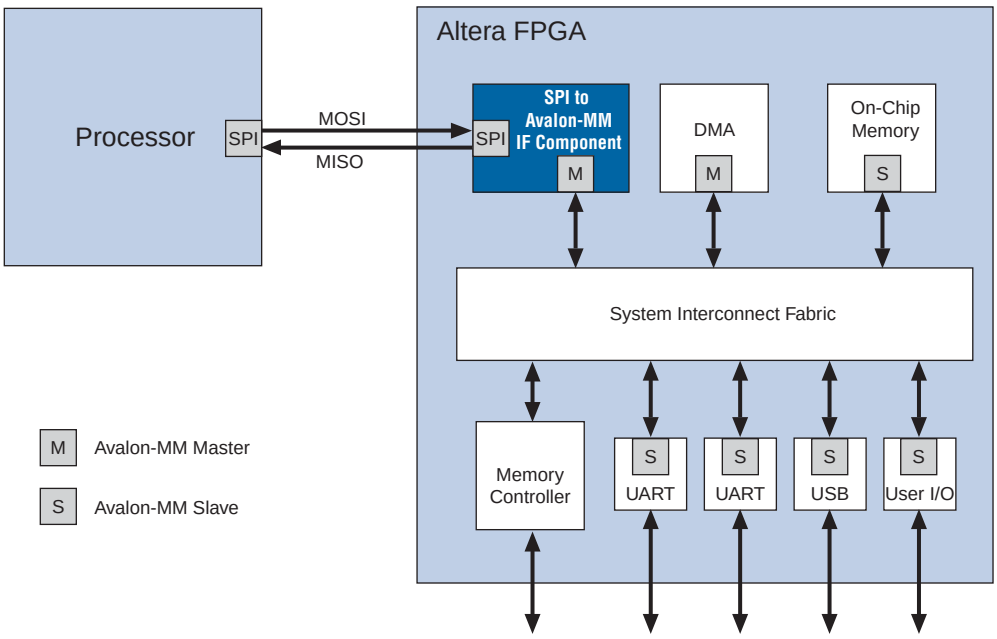
For more information, refer to *AN223: PCI-to-DDR SDRAM Reference Design*.

Serial Protocol Interface (SPI)

The SPI Slave to Avalon Master Bridge component provides a simple connection between processors and SOPC Builder systems through a four-wire industry standard serial interface. Host systems can initiate Avalon-MM transactions by sending encoded streams of bytes through the core's serial interface. The core supports read and write transactions to the SOPC Builder system for memory access and peripheral expansion.

The SPI Slave to Avalon Master Bridge is an SOPC Builder-ready component that integrates easily into any SOPC Builder system. Processors that include an SPI interface can easily encapsulate Avalon-MM transactions for reads and writes using the protocols outlined in the *SPI Slave/JTAG to Avalon Master Bridge Cores* chapter of the *Embedded Peripherals IP User Guide*.

Figure 10–8. Example System with SPI to Avalon-MM Interface Component



Details of each protocol layer can be found in the following chapters of the *Embedded Peripherals IP User Guide*:

SPI Slave/JTAG to Avalon Master Bridge Cores—Provide a connection from an external host system to an SOPC Builder system. Allow an SPI master to initiate Avalon-MM transactions.

Avalon-ST Bytes to Packets and Packets to Bytes Converter Cores—Provide a connection from an external host system to an SOPC Builder system. Allow an SPI master to initiate Avalon-ST transactions.

Avalon Packets to Transactions Converter Core—Receives streaming data from upstream components and initiates Avalon-MM transactions. Returns Avalon-MM transaction responses to requesting components.

The SPI Slave to Avalon Master Bridge Design Example demonstrates SPI transactions between an Avalon-MM host system and a remote SPI system.

Custom Bridge Interfaces

Many bus protocols can be mapped to the system interconnect fabric either directly or with some custom bridge interface logic to compensate for differences between the interface standards. The Avalon-MM interface standard, which SOPC Builder supports, is a synchronous, memory-mapped interface that is easy to create custom bridges for.

If required, you can use the component editor available in SOPC Builder to quickly define a custom bridge component to adapt the external processor bus to the Avalon-MM interface or any other standard interface that is defined in the *Avalon Interfaces Specifications*. The **Templates** menu available in the component editor includes menu items to add any of the standard Avalon interfaces to your custom bridge. You can then use the **Interfaces** tab of the component editor to modify timing parameters including: **Setup**, **Read Wait**, **Write Wait**, and **Hold** timing parameters, if required.

For more information about the component editor, refer to the *Component Editor* chapter in the *SOPC Builder User Guide*.

The Avalon-MM protocol requires that all masters provide byte addresses. Consequently, it may be necessary for your custom bridge component to add address wires when translating from the external processor bus interface to the Avalon-MM interface. For example, if your processor bus has a 16-bit word address, you must add one additional low-order address bit. If processor bus drives 32-bit word addresses, you must add two additional, low-order address bits. In both cases, the extra bits should be tied to 0. The external processor accesses individual byte lanes using the byte enable signals.

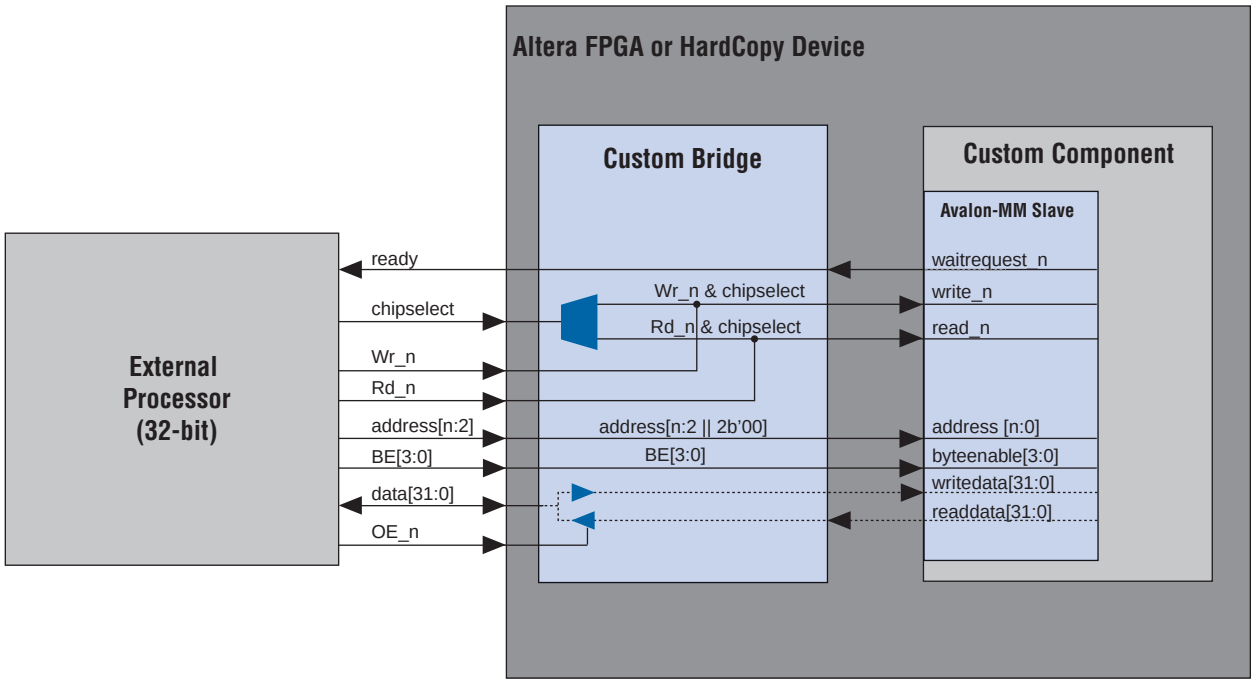
Consider the following points when designing a custom bridge to interface between an external processor and the Avalon-MM interface:

- The processor bus signals must comply or be adapted with logic to comply with the signals used for transactions, as described in the *Avalon Interfaces Specifications*.
- The external processor must support the Avalon `waitrequest` signal that inserts wait-state cycles for slave components
- The system bus must have a bus reference clock to drive SOPC Builder interface logic in the FPGA.
- No time-out mechanism is available if you are using the Avalon-MM interface.

- You must analyze the timing requirements of the system. You should perform a timing analysis to guarantee that all synchronous timing requirements for the external processor and Avalon-MM interface are met. Examine the following timing characteristics:
  - Data t_{SU}, t_H, and t_{CO} times to the bus reference clock
  - f_{MAX} of the system matches the performance of the bus reference clock
  - Turn-around time for a read-to-write transfer or a write-to-read transfer for the processor is well understood

If your processor has dedicated read and write buses, you can map them to the Avalon-MM `readdata` and `writedata` signals. If your processor uses a bidirectional data bus, the bridge component can implement the tristate logic controlled by the processor's output enable signal to merge the `readdata` and `writedata` signals into a bidirectional data bus at the pins of the FPGA. Most of the other processor signals can pass through the bridge component if they adhere to the Avalon-MM protocol. Figure 10–9 illustrates the use of a bridge component with a 32-bit external processor.

Figure 10–9. Custom Bridge to Adapt an External Processor to an Avalon-MM Slave Interface



For more information about designing with the Avalon-MM interface refer to the *Avalon Interfaces Specifications*.

Conclusion

Altera offers a variety of components that you can use to connect an FPGA to an external processor. With most of these components, you can choose either the SOPC Builder or MegaWizard Plug-In Manager design flow. You can also build your own custom interface to an external processor. By using the Avalon-MM interface in SOPC Builder, you can easily extend system capabilities for processors by taking advantage of the SOPC Builder library of components.

Document Revision History

Table 10–3 shows the revision history for this document.

Table 10–3. Document Revision History

Date	Version	Changes
July 2011	1.1	Updated references.
February 2009	1.0	Initial release.