DS-N28162004-10.0 Data Sheet

Performance Benchmarks Overview

This data sheet lists the performance and logic element (LE) usage for the Nios® II soft processor and peripherals. The Nios II soft processor is configurable and designed for implementation in Altera® FPGAs. The following Nios II processors were used for these benchmarks:

- Nios II/f—The Nios II/f "fast" processor is designed for high performance while presenting the most configuration options which are unavailable in the other Nios II processors.
- Nios II/s—The Nios II/s "standard" processor is designed for small size while maintaining moderate performance.
- Nios II/e—The Nios II/e "economy" processor is designed for the smallest possible processor size while providing adequate performance.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise.

Results may vary slightly depending on the version of the Quartus® II software, the version of the Nios II processor, and the target device. Also, any changes to the system logic design might change the performance and LE usage. All results are generated using Qsys-based designs; with the exception of Stratix III, Cyclone III LS, and Cyclone III devices, which are generated using SOPC Builder-based designs.

Table 1 and Table 2 list the f_{MAX} and millions of instructions per second (MIPS) for a system with the following components:

- Nios II processor with JTAG debug module
- JTAG UART
- 64 kilobytes (KB) on-chip memory (Cyclone® designs use one megabyte [MB] of off-chip SDR SDRAM)
- Avalon® Memory-Mapped (Avalon-MM) pipeline bridge
- Timer

The MIPS reports were obtained using the MIPS* (*Dhrystones 2.1 benchmark). You can download the Dhrystones 2.1 benchmark software from the Nios II Embedded Processor Design Examples page on the Altera website. For more information about the Dhrystones 2.1 benchmark software, refer to the **readme.txt** file which is included in the Dhrystones 2.1 benchmark design example.

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The Fast design example illustrates a system that has all the components listed. You can download the Fast design example from the Nios II Embedded Processor Design Examples page on the Altera website. For more information about the Fast design example, refer to the **readme.txt** file which is included in the Fast design example.

Table 1 lists the f_{MAX} values for the different types of Nios II processors.

Table 1. f_{MAX} for Nios II Processor System (MHz) (1)

Device Family	Device Used	Nios II/f	Nios II/s	Nios II/e
Stratix® V	5SGXEA7N2F45C1	310	300	340
Stratix IV	EP4S100G5H40I1	240	230	290
Stratix III	EP3SL150F1152C2	290	230	340
Cyclone V	5CGXFC7D6F31C6	160	140	200
Cyclone IV GX	EP4CGX30CF19C6	160	130	170
Cyclone III LS (2)	EP3CLS70F484C7	135	100	140
Cyclone III (2)	EP3C40F324C6	175	145	215
Arria® V GZ	5AGZME7K2F40C3	280	250	320
Arria V	5AGXFB5K4F40I3	160	180	190
Arria II GX	EP2AGX260FF35I3	170	170	300

Notes to Table 1:

(1) Results were generated using push button Analysis, Synthesis and Fitter settings in the Quartus II software.

(2) When comparing Cyclone III LS and Cyclone III results in Table 1, note that a speed grade 6 device was used for the Cyclone III device, whereas a speed grade 7 device was used for the Cyclone III LS device.

Table 2 lists the MIPS values for the different types of Nios II processors.

Table 2. MIPS for Nios II Processor System (1), (2)

Device Family	Device Used	Nios II/f	Nios II/s	Nios II/e
Stratix V	5SGXEA7N2F45C1	350	192	51
Stratix IV	EP4S100G5H40I1	271	147	43
Stratix III	EP3SL150F1152C2	340	140	48
Cyclone V	5CGXFC7D6F31C6	180	89	30
Cyclone IV GX	EP4CGX30CF19C6	181	83	26
Cyclone III LS	EP3CLS70F484C7	153	64	22
Cyclone III	EP3C40F324C6	195	90	30
Arria V GZ	5AGZME7K2F40C3	316	160	48
Arria V	5AGXFB5K4F40I3	180	115	28
Arria II GX	EP2AGX260FF35I3	192	108	45
Arria GX	EP1AGX60CF484C6	150	65	25

Notes to Table 2:

(1) Results were generated using push button Analysis, Synthesis, and Fitter settings in the Quartus II software.

(2) All the MIPS results are based on estimations.

Table 3 lists the ratio of MIPS over system clock (MIPS/MHz).

Table 3. MIPS/MHz Ratio for Nios II Processor System on Various Device Families

Device Family	Nios II/f	Nios II/s	Nios II/e
Stratix V	1.13	0.64	0.15
Stratix IV	1.13	0.64	0.15
Stratix III	1.183	0.611	0.138
Cyclone V	1.13	0.64	0.15
Cyclone IV GX	1.13	0.64	0.15
Cyclone III LS	1.13	0.64	0.15
Cyclone III	1.109	0.604	0.138
Arria V GZ	1.13	0.64	0.15
Arria V	1.13	0.64	0.15
Arria II GX	1.13	0.64	0.15

Table 4 through Table 6 list the LE usage for the Nios II processor cores and most of the common peripherals for Altera devices.

The resource utilization results were generated using moderate Analysis and Synthesis settings or Fitter settings in the Quartus II software. These results represent typical results. Your results may vary.

Table 4 lists the LE usage for Stratix V, Stratix IV and Stratix III devices.

Table 4. LE Usage for Nios II Processor Cores and Peripherals—Stratix V, Stratix IV and Stratix III Devices

Processor Core / Peripheral	Stratix V (ALMs)	Stratix IV (ALUTs)	Stratix III (ALUTs)
Nios II/f (1)	895	1,325	1,020
Nios II/s (2)	650	985	800
Nios II/e (3)	445	690	520
Nios II JTAG debug module	140	170	110
UART	65	110	40
JTAG UART	70	115	115
RAM Controller	3,000 (4)	4,000	310
Timer	80	95	120

Notes to Table 4:

(1) The Nios II/f processor used has 512-byte instruction and data caches, and no hardware multiplier.
(2) The Nios II/s processor used has a 512-byte instruction cache, no data cache, and no hardware multiplier.
(3) The Nios II/e processor used has no instruction or data caches, and no hardware multiplier.
(4) The RAM controller for this device is based on DDR3 SDRAM Controller with UniPHY.

Table 5 lists the LE usage for Cyclone IV GX, Cyclone III LS, and Cyclone III devices.

Table 5. LE Usage for Nios II Processor Cores and Peripherals—Cyclone V, Cyclone IV GX, Cyclone III LS, and Cyclone III Devices

Processor Core / Peripheral	Cyclone V (ALMs)	Cyclone IV GX	Cyclone III LS	Cyclone III (LEs)
Nios II/f (1)	1,050	2,065	1,790	1,800
Nios II/s (2)	785	1,915	1,340	1,300
Nios II/e (3)	420	1,080	690	650
Nios II JTAG debug module	140	335	290	250
UART	70	150	130	75
JTAG UART	70	160	160	170
RAM Controller	2,595	435	360	420
Timer	80	145	150	150

Notes to Table 5:

(1) The Nios II/f processor used has 512-bytes instruction and data caches, and no hardware multiplier.
(2) The Nios II/s processor used has 512-bytes instruction, no data caches and hardware multiplier.
(3) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.

Table 6 lists the LE usage for Arria V GZ, Arria V, and Arria II GX devices.

Table 6. LE Usage for Nios II Processor Cores and Peripherals—Arria V GZ, Arria V, and Arria II GX Devices

Processor Core / Peripheral	Arria V GZ (ALMs)	Arria V (ALMs)	Arria II GX (ALUTs)
Nios II/f (1)	895	990	1,355
Nios II/s (2)	640	710	1,045
Nios II/e (3)	435	420	730
Nios II JTAG debug module	140	135	170
UART	60	60	100
JTAG UART	65	65	115
RAM Controller	2,740	2,595 (4)	325
Timer	75	75	90

Notes to Table 6:

(1) The Nios II/f processor used has 512-bytes instruction and data caches, and no hardware multiplier.
(2) The Nios II/s processor used has 512-bytes instruction, no data caches and hardware multiplier.
(3) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.
(4) The RAM controller for this device is based on DDR3 SDRAM Controller with UniPHY.

Additional performance benchmarking information for the Nios II processor can be found at the following links:

- For more information about the Nios II interrupt latency performance, refer to the *Exception Handling* chapter of the *Nios II Software Developer's Handbook*.
- For more information about the Nios II floating-point custom instruction performance, refer to the *Using Nios II Floating-Point Custom Instructions Tutorial*.
- For more information about the Nios II networking applications performance, refer to *AN440: Accelerating Nios II Networking Applications*.

Document Revision History

Table 7 shows the revision history for this document.

Table 7. Document Revision History (Part 1 of 2)

Date	Version	Changes
November 2013	10.0	■ Removed information for devices that Altera no longer supports: Arria, Cyclone, Cyclone II, Stratix, Stratix II, and all HardCopy series. ■ Updated performance and LE usage for Arria II GX, Arria V, Arria V GZ, Stratix IV, and Stratix V devices with the Quartus II version 13.1 software. ■ Added performance and LE usage for Cyclone V devices with the Quartus II version 13.1 software.
July 2013	9.0	■ Measured performance and LE usage for Stratix V and Arria V devices with the Quartus II version 13.0 software ■ Updated new information for Stratix V and Arria V devices. ■ Added new information for Arria V GZ devices. ■ Removed information for Cyclone V devices.
December 2012	8.0	■ Measured performance and LE usage with the Quartus II version 12.1 software and the Nios II version 12.1 processor. ■ Added new information for Cyclone V and Arria V devices. ■ Updated all tables with new data.
June 2011	7.0	■ Measured performance and LE usage with the Quartus II version 11.0 software and the Nios II version 11.0 processor. ■ Updated all tables with new data.
July 2010	6.0	■ Measured performance and LE usage with the Quartus II version 13.0 software and the Nios II version 10.0 processor. ■ Rearranged the logic element usage for Nios II processor cores and peripherals for HardCopy IV, HardCopy III, HardCopy II, HardCopy Stratix from table 5 to table 6. ■ Added new information for Stratix V device. ■ Updated all tables with new data.
February 2010	5.0	■ Measured performance and LE usage with the Quartus II version 9.1 software and the Nios II version 9.1 processor. ■ Added new information for the Cyclone III LS, Cyclone IV GX, and HardCopy IV devices. ■ Updated information for Arria II GX devices. ■ Updated Table 1, Table 2, Table 3, Table 5, and Table 6 with new data.
June 2009	4.0	■ Measured performance and LE usage with the Quartus II version 9.0 SP1 software and the Nios II version 9.0 SP1 processor. ■ Added information for the HardCopy III, Arria II GX, and Arria GX devices. ■ Updated Tables 1 and 2 with new data. ■ Added Table 6.

Table 7. Document Revision History (Part 2 of 2)

Date	Version	Changes
July 2008	3.0	■ Measured performance and LE usage with the Quartus II version 8.0 software and the Nios II version 8.0 processor. ■ Added information for the Stratix IV device. ■ Added links for additional information on Nios II benchmark performance. ■ Updated Tables 1, 2, 4 and 5 with new data. ■ Added Table 3.
August 2007	2.0	■ Measured performance and LE usage with the Quartus II version 6.1 software and the Nios II version 6.1 processor. ■ Added information for the Stratix III, HardCopy II, and Cyclone III devices. ■ Updated Tables 1, 2, and 3 with new data.
October 2004	1.0	Initial release.