Implementing the CPRI Protocol Using the Deterministic Latency Transceiver PHY IP Core

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This application note describes the implementation of a deterministic latency PHY that complies with the Common Public Radio Interface (CPRI) protocol for a 6144 Mbps CPRI design in Altera® Arria® V, Cyclone® V, and Stratix® V devices with transceivers. It also describes the transceiver configuration and clocking scheme to achieve the deterministic latency functional mode.

Note: The reconfiguration scheme and design example included in this application note is limited to Arria V GX devices where the maximum data rate is 6144 Mbps and no ATX PLL discussion is involved.

Introduction to the CPRI Specification

The CPRI specification defines the interface of radio base stations between the radio equipment controller (REC) and the radio equipment (RE). The physical layer supports both the electrical interface (for example, traditional radio base stations) and the optical interface (for example, radio base stations with remote radio head). The scope of the CPRI specification is restricted to the link interface only, which is basically a point-to-point interface. Such a link has all the features necessary to enable a simple and robust usage of any given REC and RE network topology, including a direct interconnection of multiport REs.

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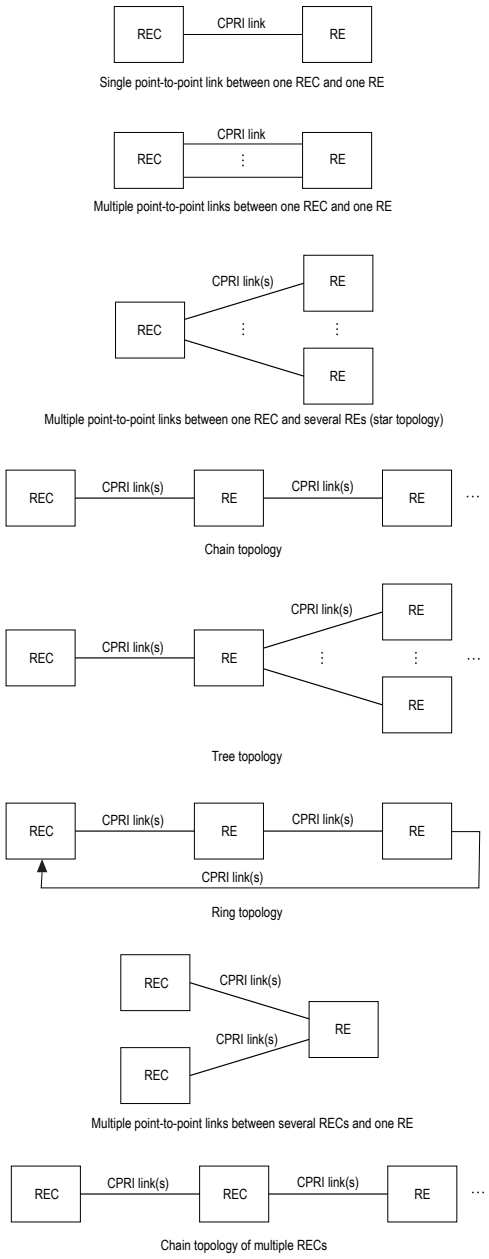
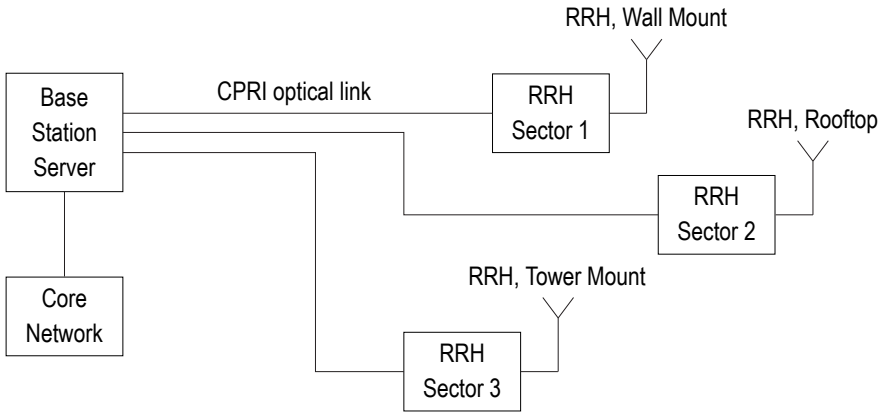
Figure 1: Basic Configuration in CPRI Topologies



The open base station architecture has evolved in parallel with the evolution of the standards to provide a flexible, cheaper, and more scalable modular environment for managing the radio access evolution. For example, the CPRI specification introduced standardized interfaces separating the base station server and the remote radio head (RRH) part of a base station by an optical fiber.

Figure 2: Example of a Distributed Open Base Station Architecture



CPRI can be used to carry the radio frequency (RF) data to the RRH in different sector cells. This architecture reduces costs for service providers because only the remote radio heads containing the RE need to be situated in environmentally challenging locations. The base stations can be centrally located in less challenging locations where footprint, climate, and availability of power are more easily managed.

Implementing Deterministic Latency for CPRI Interfaces

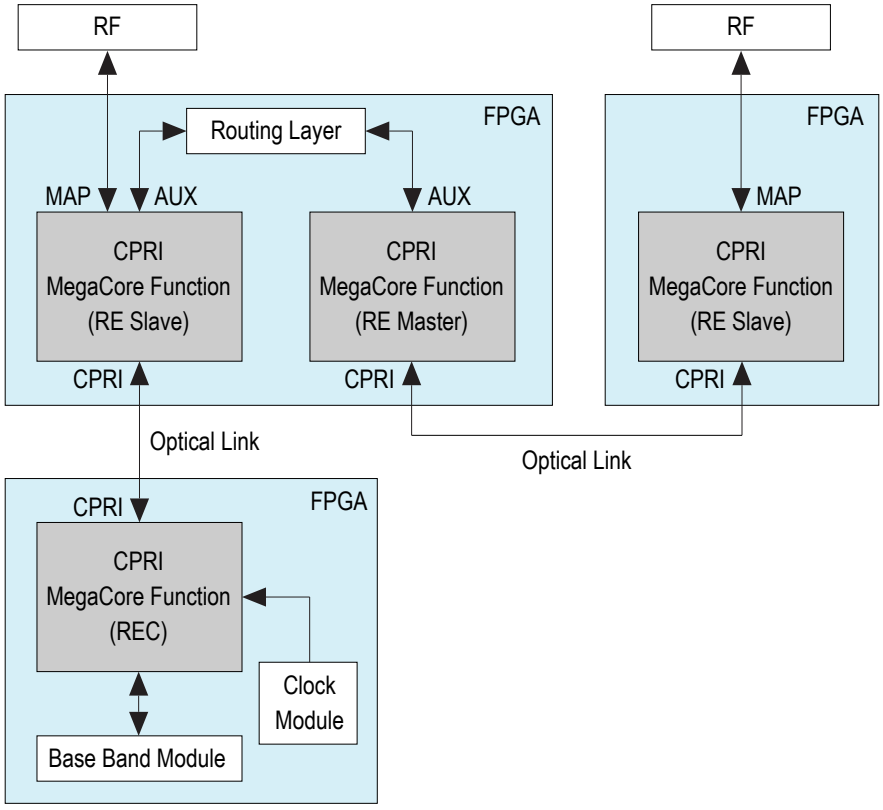
Deterministic latency PHY IP core supports many industry-standard protocols that require deterministic latency, including the following protocols:

- CPRI
- ORI
- IEEE 1588
- Open Base Station Architecture Initiative (OBSAI)
- Custom deterministic latency protocols

Deterministic latency PHY IP is supported for Arria V, Cyclone V, and Stratix V devices in the Quartus® II software.

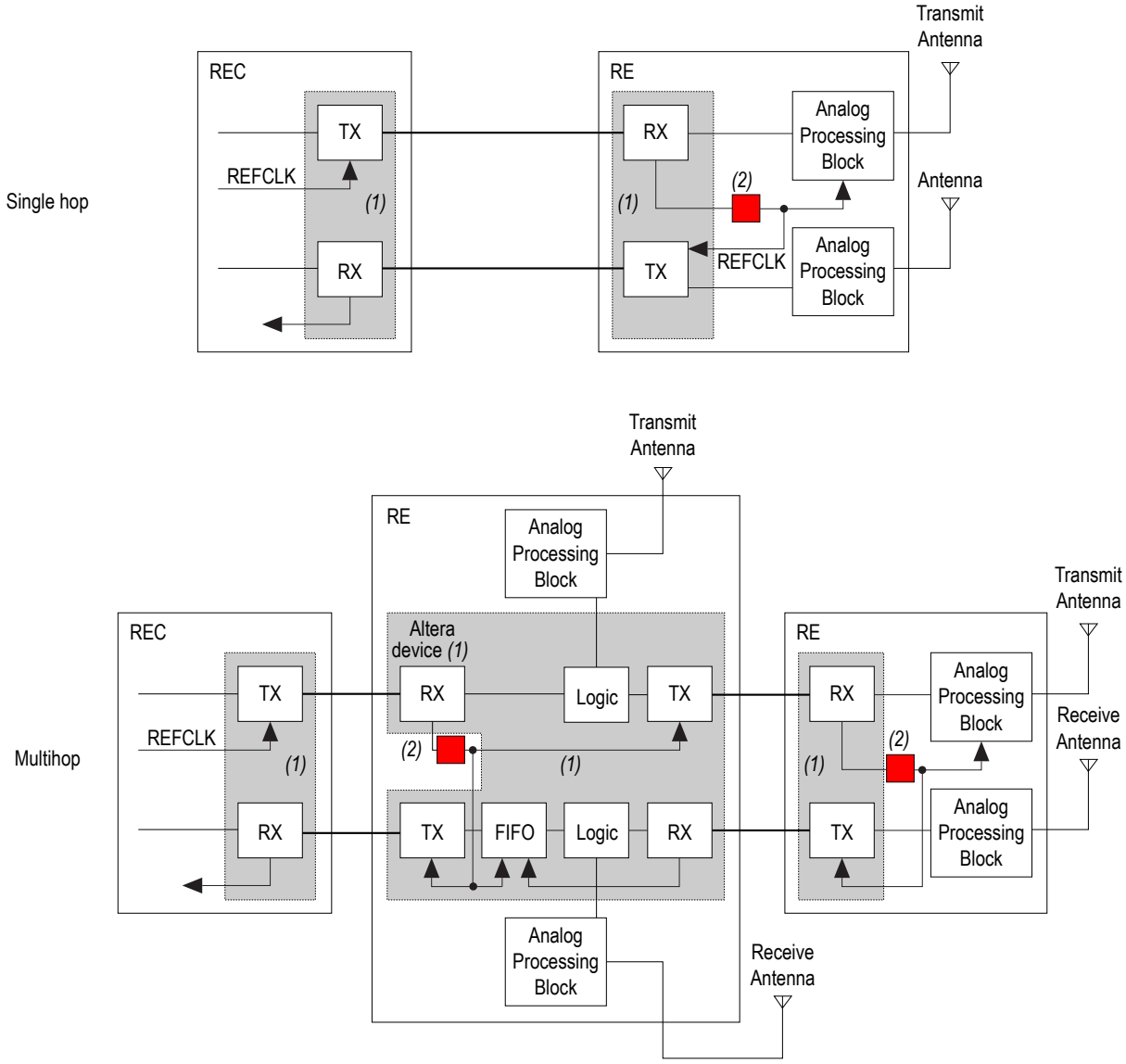
CPRI interface is a high-speed serial interface developed for the cellular phone network REC to uplink and downlink data from available remote RE.

Figure 3: Typical CPRI Application on Devices



With high bandwidth, data can be uplinked or downlinked from multiple antennas. Multiple REs can be chained to a single REC (multihop).

Figure 4: Single Hop and Multihop Connections



Notes:
1. Arria V, Cyclone V, and Stratix V devices.
2. External cleanup PLL or VCXO

To avoid transmission interference in time division multiplexed systems, every radio in a cell network requires accurate delay estimates with minimal delay uncertainty. Otherwise, transmission interference can occur in systems such as time-division multiple-access (TDMA), global system for mobile communications (GSM), or code division multiple access (CDMA), in which multiple radios share a common frequency. Lower delay uncertainty is always desired for increased spectrum usage efficiency and bandwidth. The Cyclone V, Arria V, and Stratix V FPGA devices are designed with features to minimize the delay uncertainty for both RECs and REs.

Related Links

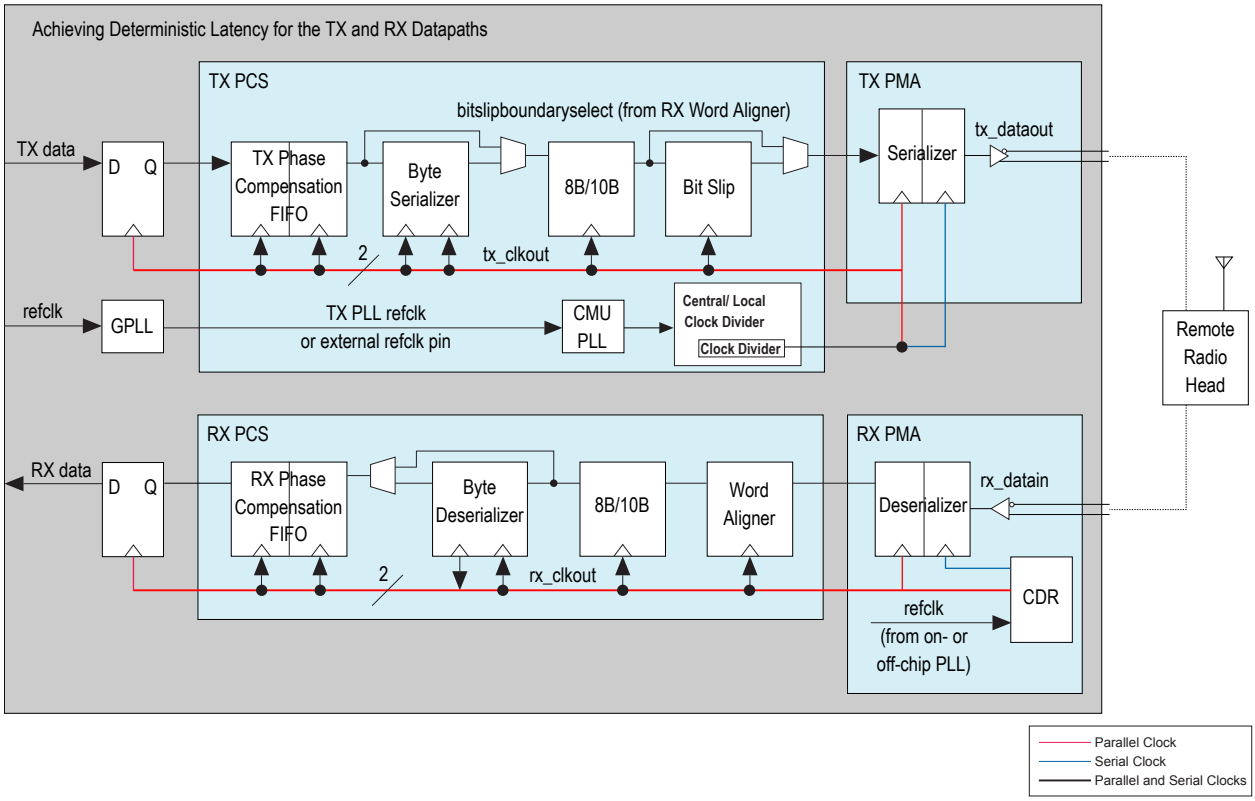
For more information on how to determine the latency through the PHY in Arria V, Cyclone V, and Stratix V devices, refer to the "Deterministic Latency PHY IP Core" chapter in the Altera Transceiver PHY IP Core User Guide.

Transceiver Support for CPRI Applications

The round trip delay accuracy requirement (R-21) of the CPRI specification requires the round-trip delay measurement accuracy, excluding the cable, to be within ±16.276 ns for single hop and multihop connections. In multihop connections, the allowed delay uncertainty is accumulated over the number of hops in the connection.

The Arria V, Cyclone V, and Stratix V devices include embedded transceivers with deterministic latency features that easily meet the delay accuracy requirements of the CPRI specification. The deterministic latency features enable you to accurately compute the transceiver datapath latencies when using the CPRI standardized interfaces.

Figure 5: Typical REC Block Diagram Implemented in Arria V Devices



For more information about the supported data rates for CPRI implementation using transceivers in the Arria V , Cyclone V, and Stratix V devices, refer to *Table 2*.

Table 1: TX and RX Standard PCS Sub-block Description when Configured in CPRI Protocol

The PCS sub-blocks are configured to support the CPRI protocol.

TX/RX Standard PCS Sub-block	Feature/Descriptions
TX and RX Phase Compensation FIFO Buffers	• The TX and RX phase compensation FIFO buffers are always in register mode. • The latency of The phase compensation FIFO buffers is always one clock cycle.

TX/RX Standard PCS Sub-block	Feature/Descriptions
Byte Serializer and Byte Deserializer	The byte serializer and byte deserializer support /1 (bypass) and /2 serialization and deserialization.
8B/10B Encoder and Decoder	Supports both enabled or disabled of the 8B/10B encoder and decoder.
Word Aligner	• Supports both deterministic latency state machine and manual alignment mode. • Allows fixed latency to be done on the receiver path. • Reduces known delay variation from the word alignment process. • Additional user logic is not required to manipulate the TX bit slipper for constant round-trip delay. • TX bit slipper used in manual alignment mode is similar to the Stratix IV/ Arria II device family.

Related Links

For more information about Arria V device support for CPRI, refer to the Arria V Transceiver Protocol Configurations chapter.

For more information about Cyclone V device support for CPRI, refer to the Cyclone V Transceiver Protocol Configurations chapter.

For more information about Stratix V device support for CPRI, refer to the Stratix V Transceiver Configurations chapter.

Data Rate Support and Channel Width Information

To support the multi-rate of CPRI at 3072 Mbps or 6144 Mbps in addition to data rates chosen from 1228.8 Mbps, 2457.6 Mbps, 4915.2 Mbps, and 9830.4 Mbps, you are required to use two separate PLLs to generate the high speed and low speed clocks. For systems that do not use 3072 Mbps or 6144 Mbps, a single PLL can be used.

Table 2: Channel Width Options for Supported Serial Data Rates

The Cyclone V device supports up to 4915.2 Mbps. Arria V and Stratix V devices support up to 9830.4 Mbps. Arria V GT device supports 9830.4 Mbps using PMA direct mode and soft PCS. For the exact device speed grade and its supported data rate, refer to the appropriate device datasheet.

Serial Data Rate (Mbps)	Channel Width (FGPA-PCS Fabric)			
	8/10-Bit-Width		16/20-Bit-Width	
	8-Bit	16-Bit	16-Bit	32-Bit
614.4	Yes	Yes	—	—
1228.8	Yes	Yes	Yes	Yes
2457.6	—	Yes	Yes	Yes
3072	—	Yes	Yes	Yes
4915.2	—	—	—	Yes
6144	—	—	—	Yes [1]

[1] Supported by Arria V GX/GT using standard PCS.

Serial Data Rate (Mbps)	Channel Width (FGPA-PCS Fabric)			
	8/10-Bit-Width		16/20-Bit-Width	
	8-Bit	16-Bit	16-Bit	32-Bit
9830.4	—	—	—	Yes [2, 3]

Note: If you need to run CPRI channel at 614.4 Mbps, you can use FPLL to generate the high speed and low speed clock in Arria V and Cyclone V devices. In Stratix V devices, you can use the TX local clock divider /8 setting to divide down the 4915.2 Mbps to support this data rate.

Refer to *Reconfiguration Scheme* on page 9 to see how the clock sources are use to support the multi-rate CPRI applications.

Backward Compatibility

This PHY IP is not directly backward compatible with ALTGX variants because of the significant change in standard interfaces.

The PHY IP bonded-mode configuration is not supported for the CPRI protocol.

Design Considerations in Creating Multi-Rate CPRI Channels Design

If you are creating CPRI designs involving multi-rate reconfiguration, note the following requirements:

- Channel Placement Restriction
- Reconfiguration Scheme
- TX PLL and Data Channel resources

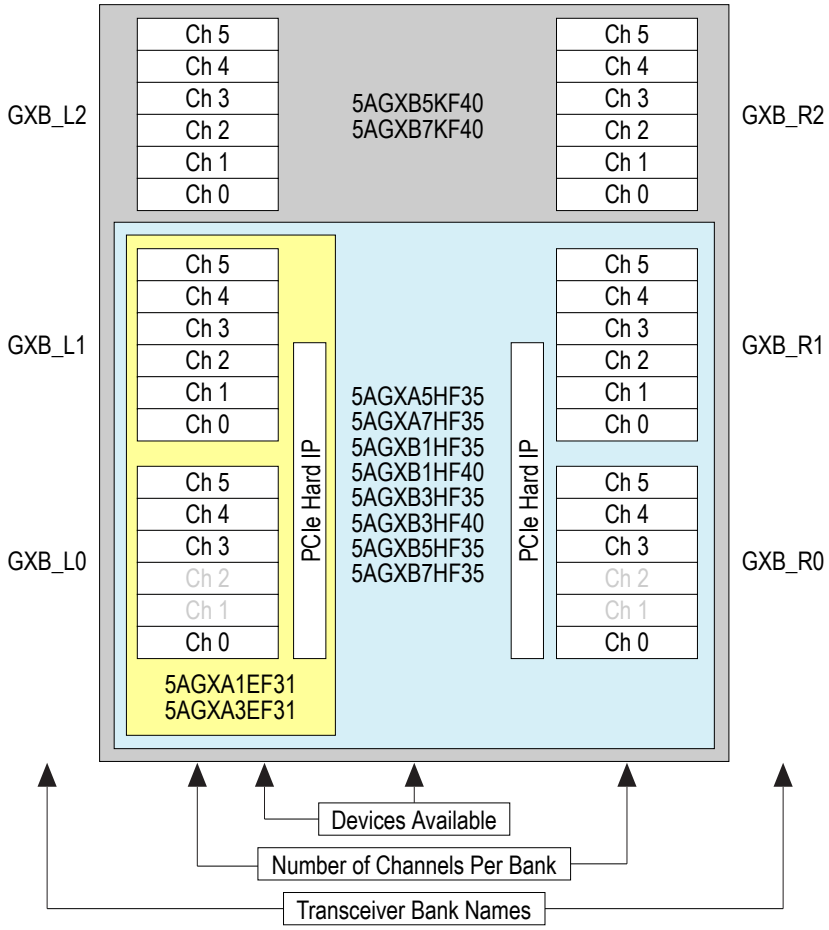
CPRI Channel Placement Restriction in Arria V GX/GT Devices

The Quartus II software has a channel placement restriction on the Arria V GX/GT device if you are implementing a 6144-Mbps CPRI channel using deterministic latency PHY IP core.

Channel placement can be in any location except for ch1 and ch2 of the lowest triplet on each side of the device (GXB_L0 and GXB_R0). This restriction is due to the physical Hard IP block (HIP) located adjacent to these channels which can cause complications in closing timing at 6144 Mbps. Cyclone V and Stratix V devices do not have this placement restriction.

[2] Supported by the Arria V GZ and Stratix V devices using standard PCS.
[3] The Arria V GT device supports CPRI 9830.4 Mbps using PMA direct mode and soft PCS with 80-bits PMA-PLD data width, and is available only in 10-Gbps channels.

Figure 6: Channel Placement Restriction for CPRI Specification in Arria V GX/GT Devices



Reconfiguration Scheme

Each CPRI channel requires independent rate change and should be reconfigured to different **data rate** at different times independently without affecting the remaining channels.

To achieve this, select at least two different clock sources in your design. The supported data rates with this approach are 6144 Mbps, 4915.2 Mbps, 3072 Mbps, 2457.6 Mbps, 1228.8 Mbps, and 614.4 Mbps.

Note: The reconfiguration scheme for CPRI channels running up to 6144 Mbps applies only to Arria V and Stratix V devices because the maximum supported data rate for Cyclone V is 5 Gbps.

To achieve independent rate change for your CPRI channels, consider the following requirements. Use the reconfiguration option to achieve the multi-rate change applications.

Reconfiguring the CPRI transmitter requires:

- Data rate division using TX local clock dividers
- Channel reconfiguration with TX PLL switching

Reconfiguring the CPRI receiver requires CDR/RX channel reconfiguration.

Reconfiguring the CPRI Transmitter Channels

Data Rate Division in TX

In the reference design, this reconfiguration option is used to showcase the rate change for data rates that are related (in multiples of /1, /2 or /4 of each other). It is accomplished by reconfiguring the TX local clock divider settings of the specific transmitter channel as in the following examples:

- From 4915.2 Mbps to 2457.6 Mbps, or 1228.8 Mbps
- From 6144 Mbps to 3072 Mbps

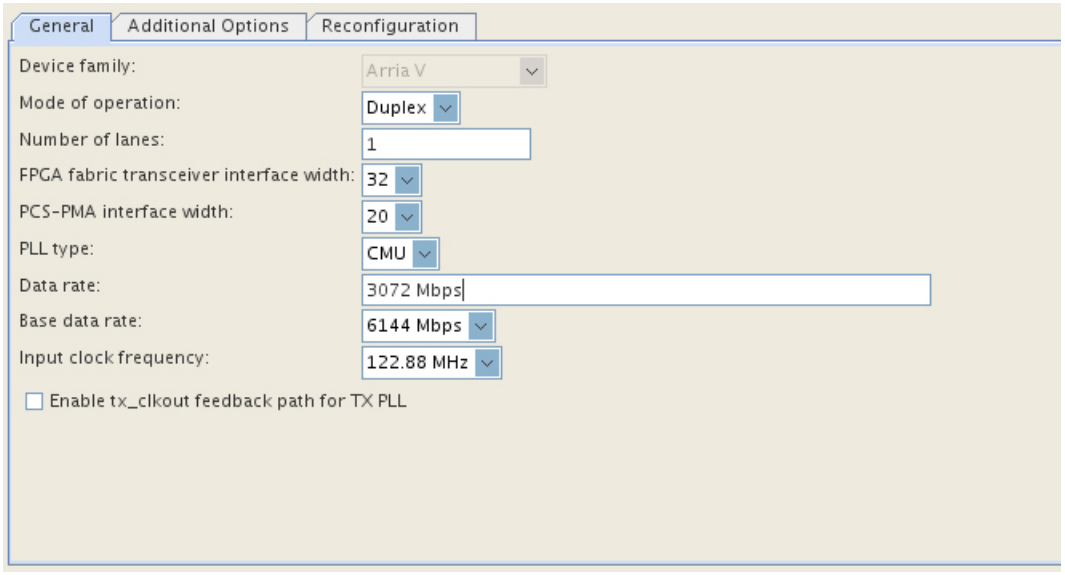
Only the Stratix V device supports the TX local clock dividers setting of /8. You can divide the **base data rate** of 9830.4 Mbps and divide down to get 1228.8 Mbps in the Stratix V device. Alternatively, you can divide down the 4915.2 Mbps to support 614.4 Mbps using this same divider setting.

The design example included in this application note only discusses the usage of /1, /2 and /4 divider settings, because /8 local divider setting is not supported in Arria V GX devices.

This mode can be enabled to share the same TX PLL and perform rate negotiation independently without affecting each other while listening to the same TX PLL.

Tip: Set the **base data rate** and **data rate** in the deterministic latency PHY IP General tab to engage the TX local clock dividers. The **base data rate** will be the data rate used for other data rates in a division of 1, 2 and 4. The **data rate** is the effective **data rate** for the channels set in this instance.

Figure 7: Base Data Rate and Data Rate Setting in Deterministic Latency PHY IP Settings



Channel Reconfiguration with TX PLL Switching

This reconfiguration option allows you to perform rate negotiation to unrelated data rates (not in multiples of /1, /2, or /4 of each other) by reconfiguring the specific transmitter channel to select clocks from another TX PLL. For example:

- From 6144 Mbps to 4915.2 Mbps
- From 4915.2 Mbps to 3072 Mbps

The design example shows that with this reconfiguration option, you need to have two clock sources in your design, generated by two TX PLLs—one with the initial **data rate** clock settings and the other with the

negotiated lower **data rate** clock settings. Reconfiguring the transmitter using this mode will not affect other channels that listen to either of the TX PLLs.

This reconfiguration option is used together with the **data rate** division in TX reconfiguration option for greater negotiation flexibility. For example:

- From 6144 Mbps to 4915.2 Mbps, then to 3072 Mbps
- From 4915.2 Mbps to 3072 Mbps, then to 2457.6 Mbps

In the design example, the following TX PLLs are used to clock the respective CPRI data rates:

- TX PLL0 to generate **data rate** cluster #1 - 4915.2 Mbps, 2457.6 Mbps and 1228.8 Mbps
- TX PLL1 to generate **data rate** cluster #2 - 6144 Mbps and 3072 Mbps

Related Links

6G CPRI Auto-rate Negotiation Design Example for Arria V GX on page 12

Reconfiguring the CPRI Receiver Channel

You can reconfigure the receiver channels by using the Channel and CMU PLL reconfiguration mode. This is a streamer-based reconfiguration mode, and it can be used to perform rate negotiation to the desired data rate by reconfiguring the CDR settings. You can do this by checking the **Allow PLL/CDR Reconfiguration** option under the Reconfiguration tab of the deterministic latency PHY IP.

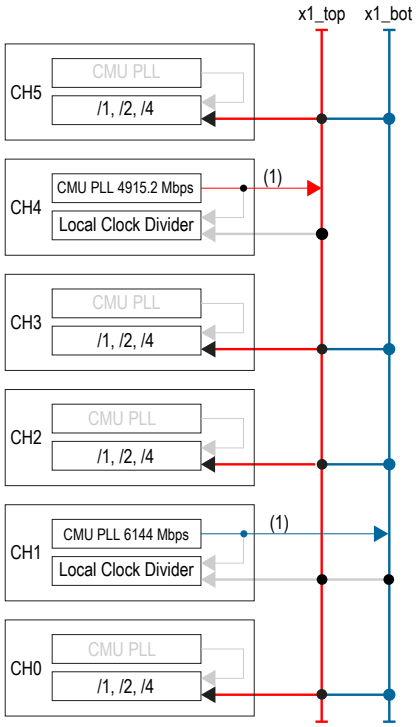
TX PLL and Data Channels Resources

An application with CPRI channel changing rate from 6144 Mbps down to 1228.8 Mbps includes the following details:

- Four CPRI duplex channels in a transceiver bank
- Switching between two TX PLLs to support two different clusters of data rates
- Engaging TX local clock dividers of /1,/2 and /4
- Using streamer-based reconfiguration to reconfigure both transmitter and receiver

Figure 8: TX PLLs, TX Local Clock Dividers, and Data Channels Resources Information for Arria V Devices

All clock lines shown carry the serial clock only.



Note:
1. You can use the same TX PLL to clock CPRI channels in other banks on the same side of the device. It will use the x6 and xN clock line to send the high speed clock to the respective CPRI channels.

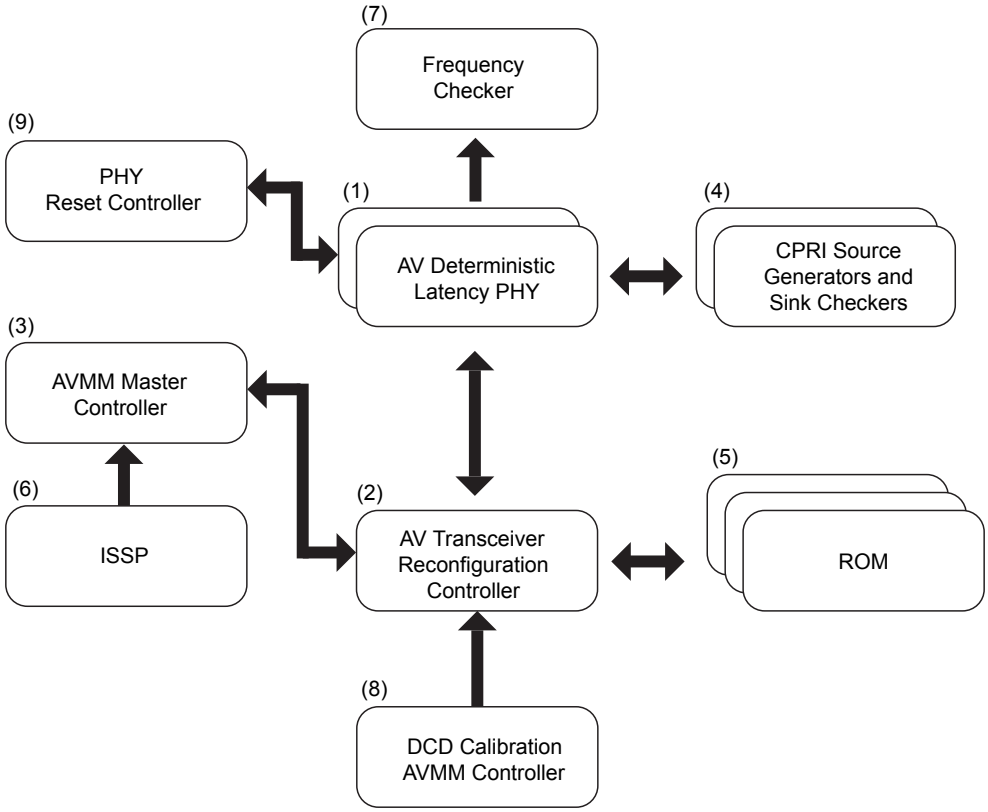
6G CPRI Auto-rate Negotiation Design Example for Arria V GX

The reconfiguration features are based on the Arria V device family.

Where necessary, any differences in terms of reconfiguration features between the device families (Arria V, Cyclone V, and Stratix V), are explained in detail.

The design example shows the rate changStratix Ve of CPRI channels from 6144 Mbps down to 1228.8 Mbps. The reconfiguration is accomplished by triggering a pulse in the design by using In-system Sources and Probes (ISSP).

Figure 9: 6G CPRI Auto-rate Negotiation Design Example Block Diagram



Legend:
1. Two deterministic latency PHY are generated by the MegaWizard Plug-in Manager for RE configuration:
   - One (x1) duplex CPRI channel
   - Two TX PLLs selected (TX PLL0 and TXPLL1)
2. Used to dynamically reconfigure both deterministic latency PHY IPs.
3. Used to control the interface to each deterministic latency PHY IP and reconfiguration controller.
4. Connected to each deterministic latency PHY:
   - cpri_src--This instance generates one CPRI K28.5 character and PRBS7 pattterns to the 32-bit `tx_parallel_data` input of the deterministic latency PHY instance.
   - cpri_sink--This instance is a frame checker to verify the correctness of the received data, which consists of one CPRI K28.5 character and PRBS7 patterns. `Atest_pass` signal from this IP shows that the CPRI verifier received correct data.
5. Four ROMs instantiated to store multi data rate MIF files for different data rates (for example: 6144 Mbps, 4915.2 Mbps, 3072 Mbps, 2457.6 Mbps, and 1228.8 Mbps).
6. Used to trigger the reconfiguration process of Ch0, Ch1.
7. This instance consists of frequency checkers that verify the frequency precision of the `tx_clkout` and `rx_clkout`.
8. AVMM master used to manually trigger the DCD calibration IP. It uses the register-based reconfiguration.
9. External PHY reset controller used to reset the CPRI channels and as a system reset.

Note: All design files referenced in this application note are located in the *original_design/source* directory contained with the `av_cpri_rate_negotiation_ref_design.zip` file.

This reference design demonstrates the functionality of the reconfiguration controller by showcasing:

- Channel reconfiguration using the streamer-based reconfiguration mode
- Duty Cycle Distortion (DCD) calibration using register-based reconfiguration

The Arria V GX FPGA Development Kit is used for this design example. Refer to the pin assignment section for the channel assignment information.

Creating the Deterministic Latency PHY IP

The design example uses the deterministic latency PHY IP as a single duplex CPRI channel.

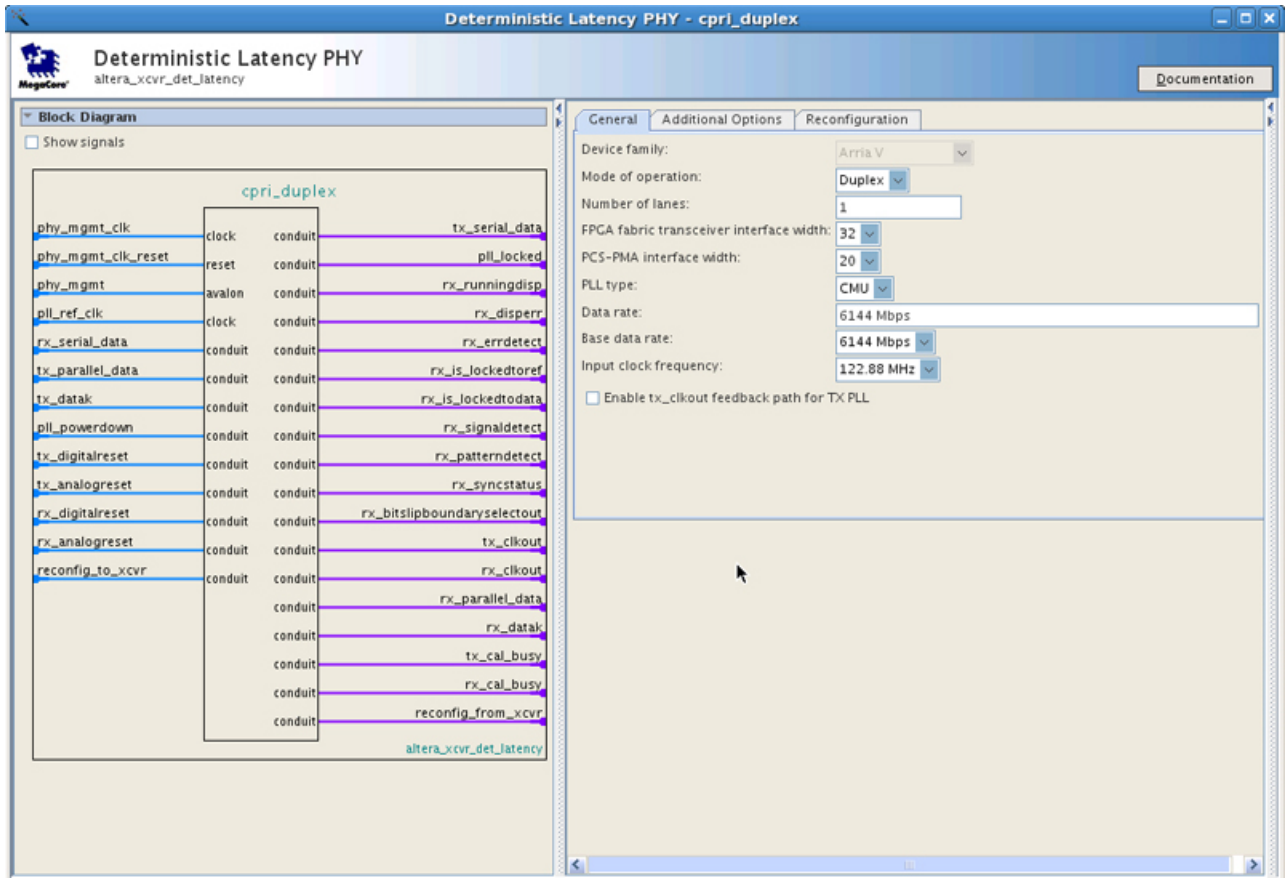
The deterministic latency PHY is created such that two transmit PLLs are used. The first transmit PLL (TX PLL 0) is configured to run at **data rate** of 4915.2 Mbps and the second transmit PLL (TX PLL 1) is configured to run at **data rate** of 6144 Mbps. With the reconfiguration controller connected you'll be able to selectively determine which transmit PLL is used.

1. Launch the Quartus II software.
2. Select Tools > MegaWizard Plug-In Manager.
3. Select Edit an existing custom Megafunction variation.
4. Press Next.
5. Browse and select the `cpri_duplex.v` file located in the *original_design/source* directory.
6. Press Next.

   The **General** tab appears first after the deterministic latency PHY IP opens in the MegaWizard Plug-In Manager. This tab contains the general settings for the deterministic latency PHY IP.

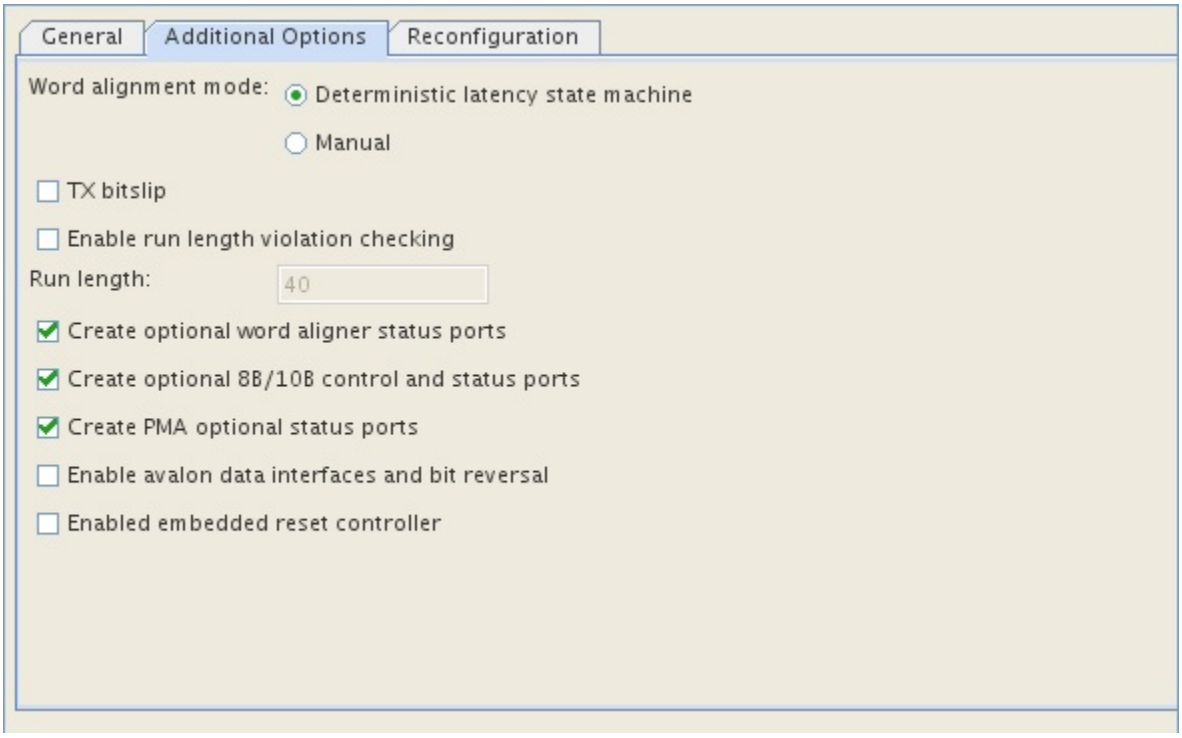
   The initial **data rate** set for the design is 6144 Mbps and uses an input reference clock frequency of 122.88 MHz.

Figure 10: General Tab of the Deterministic Latency PHY IP



7. Click the **Additional Options** tab in MegaWizard Plug-In Manager.
   This tab contains optional ports and features that can be enabled.

Figure 11: Additional Options Tab of the Deterministic Latency PHY IP



8. Click the **Reconfiguration** tab in the MegaWizard Plug-In Manager.
   This tab contains all the reconfiguration features in the deterministic latency PHY IP. To change the **data rate**, this design needs to specify two transmit PLLs. The first transmit PLL is used for generating the data rates of 4915.2 Mbps, 2457.6 Mbps, and 1288.8 Mbps. The second transmit PLL is used for generating the data rates of 6144 Mbps and 3072 Mbps. The reference clock setting is the same for both data rates.

Figure 12: TX PLL 0 Setting in the Deterministic Latency PHY IP

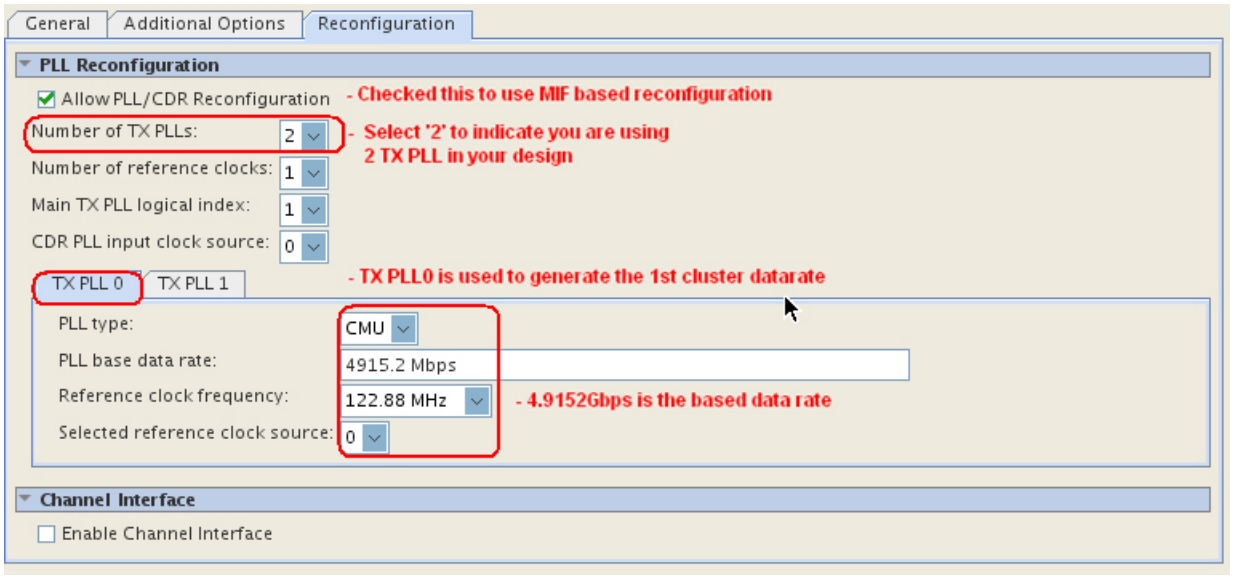
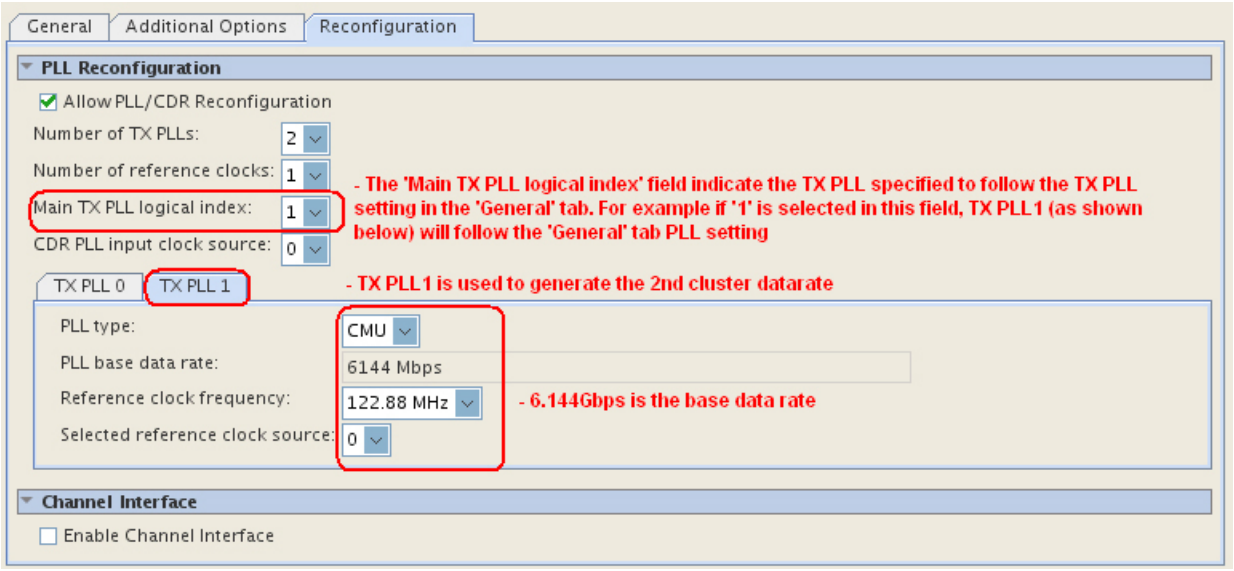


Figure 13: TX PLL 1 Setting in the Deterministic Latency PHY IP



When the **main TX PLL** logical index setting is **1**, the parameters in the TX PLL1 section are not editable because the main TX PLL logical index indicates the TX PLL settings/parameters specified to follow the TX PLL specified in the general tap. In this case, the data rate is set to 6144 Mbps with a reference clock of 122.88 MHz.

The parameters in TX PLL0 section specify the values for the second transmit PLL. For this design the transmit PLL generates a fast clock for channel running at 4915.2 Mbps with a reference clock frequency of 122.88 MHz.

9. Click Finish in the MegaWizard Plug-In Manager.

Related Links

For more information on the deterministic latency PHY IP, refer to the Altera Transceiver PHY IP Core User Guide.

Creating the Reconfiguration Controller

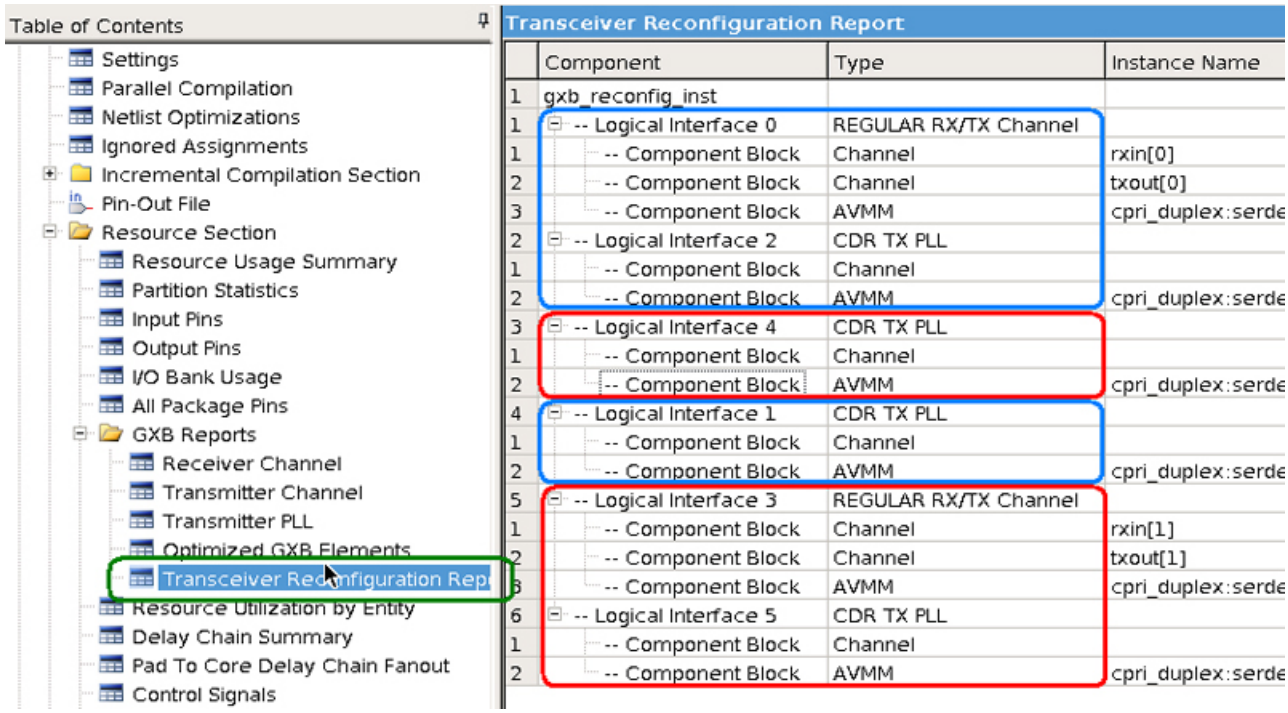
The reconfiguration controller is used to control the dynamic reconfiguration of all Altera Transceiver PHY IPs. This procedure shows you how to setup the reconfiguration controller to perform streamer-based and register-based reconfiguration.

1. Launch the Quartus II software.
2. Select Tools > MegaWizard Plug-In Manager.
3. Select **Edit an existing custom Megafunction variation**.
4. Press Next.
5. Browse and select the `gxb_reconfig.v` file located in the *original_design/source* directory.

   The deterministic latency PHY IP created in the previous section requires six reconfiguration interfaces because each deterministic latency PHY IP uses a single channel and in turn, each channel has three reconfiguration interfaces: the RX/TX channels, TX PLL, and the CDR. Because there are two deterministic latency PHY IP, there will be six reconfiguration interfaces in total.

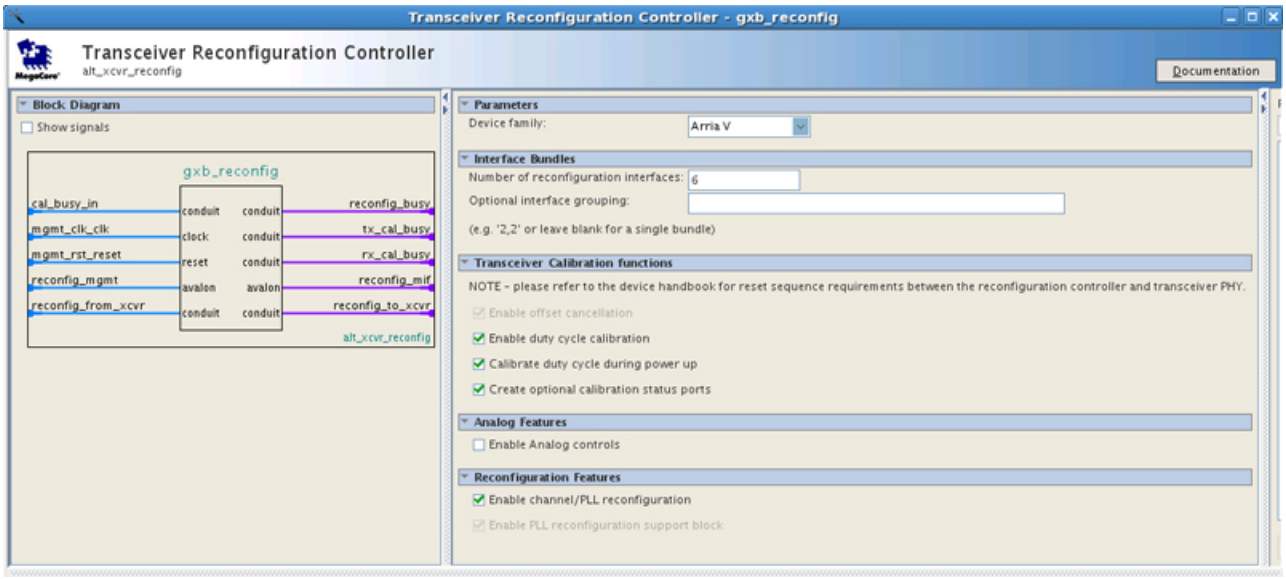
   The Quartus II fitter report sections show the reconfiguration interface information under **GXB Reports > Transceiver Reconfiguration Report.**

Figure 14: Transceiver Reconfiguration Report



There is no need to specify a value in the optional grouping field.

Figure 15: Transceiver Reconfiguration Controller Settings



The offset cancellation process runs automatically after power up mode. Duty cycle distortion (DCD) calibration is used for duty cycle distortion caused by clock network skew. DCD calibration can be turned on during power up or triggered manually during user mode, whenever necessary. For this design example, you can select all options under the transceiver calibration function. No analog reconfiguration controls are selected for this design example.

Note: The design example only shows the Arria V GX device; however, the Cyclone V device shares the same transceiver calibration feature. TheArria V GZ and Stratix V devices have a different calibration function support.

The Channel/PLL reconfiguration feature must be enabled. Selecting this box indicates that you are going to use streamer-based reconfiguration to reconfigure the CPRI channels.

After all parameters have been specified you are ready to generate the reconfiguration controller.

6. Click Finish in the MegaWizard Plug-In Manager.

Related Links

Refer to Altera transceiver PHY IP User Guide for the supported calibration features.

Creating a ROM Containing the MIF for Reconfiguration

Dynamic reconfiguration of the deterministic latency PHY can be performed using one of two methods: register-based and streamer-based.

The register-based reconfiguration is carried out by writing to a specific set of memory-mapped registers in the Reconfiguration Controller. For example, to manually trigger the DCD calibration IPs you can write to the specific memory-mapped registers in the reconfiguration controller to execute the DCD calibration process.

Note: Only the Arria V GX/GT and Cyclone V GT devices need DCD calibration IP. DCD calibration IP in the transceiver reconfiguration controller is not supported in Arria V GZ and Stratix V devices.

The streamer-based reconfiguration is accomplished by streaming a MIF, which contains the reconfiguration data, to the reconfiguration controller.

It is recommended that you have two separate designs when generating a MIF for reconfiguration. The first design, or the original design, is the functional design that is used to generate the programming file (SOF) for the Arria V device. The second design, or MIF design, contains the deterministic latency PHY IP settings for reconfiguration. The MIF design is purely used to generate the MIF for the original design and nothing else. This procedure describes how to generate the MIF design used in the sample design. This helps you avoid long compilation time and also does not affect your original deterministic latency PHY IP instantiation in your original design (static design).

Note: Two design directories should be used to compile the original design and the MIF design. This prevents inadvertently deleting or modifying design files.

The MIF design is simply the original design with different settings specified for the deterministic latency PHY IP. In the original design the initial **data rate** is set to 6144 Mbps; however, after MIF reconfiguration, we change the data rates to 4915.2 Mbps, 3072 Mbps, 2457.6 Mbps, and finally 1228.58 Mbps. The MIF files can be generated by changing the deterministic latency PHY IP settings. Only the settings contained on the General and Reconfiguration tabs will be changed. These steps detail the changes that need to be made to the reconfiguration controller.

1. Launch the Quartus II software.
2. Select Tools > MegaWizard Plug-In Manager.
3. Select Edit an existing custom Megafunction variation.
4. Press Next.
5. Browse and select the `cpri_duplex.v` file located in the *mif_design/source* directory.

The initial **data rate** for the MIF design needs to be set to 6144 Mbps. When generating the MIF files, you need to select the **Allow PLL/CDR Reconfiguration** option to enable MIF-based reconfiguration. Use the information in *Table 3* to generate the MIF files.

6. Click the Reconfiguration tab in the MegaWizard Plug-In Manager.
7. Click Finish in the MegaWizard Plug-In Manager.
   After all parameters have been specified, you can generate the deterministic latency PHY IP for the MIF design.

Table 3: MIF File Generation and Deterministic Latency PHY IP Configurations

The rest of the deterministic latency PHY IP settings not mentioned in this table remains the same throughout all MIF file generation.

MIF #	MIF Files to be Generated	General Tab		Reconfiguration Tab			Hardware Setting
		Data Rate (Mbps)	Base Data Rate (Mbps)	TX PLL 0 PLL Base Data Rate (Mbps)	TX PLL1 PLL Base Data Rate (Mbps)	Main TX PLL Logical Index	Dividers setting
1	6144 Mbps	6144	6144	4915.2	6144	1	/1
2	4915.2 Mbps	4915.2	4915.2	4915.2	6144	0	/1
3	3072 Mbps	3072	6144	4915.2	6144	1	/2
4	2457.6 Mbps	2457.6	4915.2	4915.2	6144	0	/2
5	1228.8 Mbps	1228.8	4915.2	4915.2	6144	0	/4

Compiling the Design

At this point two designs exist: the original design and the MIF design. The first design to compile will be the MIF design. The MIF design is compiled first because the MIF generated will be used by the original design. Specifically, the MIF generated by the MIF design is used in the original design to configure from one data rate to another. This procedure describes how to perform a design compilation.

1. Open the MIF project in the Quartus II software.
2. Select Processing > Start Compilation.
   After a successful compilation, a *reconfig_mif* directory will be created in the MIF design's project directory. The following are the MIF files used for each data rate:
   - 6144 Mbps - `gxb_cpri_6g_inst_channel.mif`
   - 4915.2 Mbps - `gxb_cpri_4g_inst_channel.mif`
   - 3072 Mbps - `gxb_cpri_3g_inst_channel.mif`
   - 2457.6 Mbps - `gxb_cpri_2g_inst_channel.mif`
   - 1228.8 Mbps - `gxb_cpri_1g_inst_channel.mif`

   The original design is compiled after the MIF design. But, before the original design is compiled, you'll need to specify the MIF created by the MIF design. The module `mif_rom<#>`, where # indicates the number, 6, 4, 3, 2, or 1, is used to store the MIF.
3. Open the original project in the Quartus II software.
4. Select Tools > MegaWizard Plug-In Manager.
5. Browse to the *original_design/source* directory and select `mif_rom<#>.v`.

6. Specify the `mif_design/reconfig_mif/gxb_cpri_6g_inst_channel.mif` file by browsing to the MIF. All parameters are the same, except you need to specify the MIF file.
7. Click Finish to generate the new `mif_rom<#>` module.
8. Repeat step *step 3* through step *step 7* for the remaining MIF files in each `mif_rom<#>` instantiated. After the MIF has been specified, the original design is ready for compilation.
9. Open the original project in the Quartus II software.
10. Select Processing > Start Compilation.
    After a successful compilation, an `a5_top.sof` file is placed in the original design directory. This SOF will be used to program the Arria V device.

Reconfiguring the CPRI Channels

There are two methods shown in the design example, which is to reconfigure the CPRI channels to different data rates and to perform manual DCD calibration:

- Using streamer-based reconfiguration mode to achieve different data rate
- Using the register-based method to manually trigger DCD calibration IP when switching to different clock network (TX PLL switch)

Related Links

For more information on the specific address map associated with the reconfiguration controller refer to the Altera Transceiver PHY IP Core User Guide.

Streaming a MIF to Perform Channel Reconfiguration

These procedures describe how to change the CPRI channel's data rate from 6144 Mbps down to 1228.8 Mbps.

You can use the ISSP module in the design example to trigger the streamer-based reconfiguration process.

The ISSP module consists of two sources:

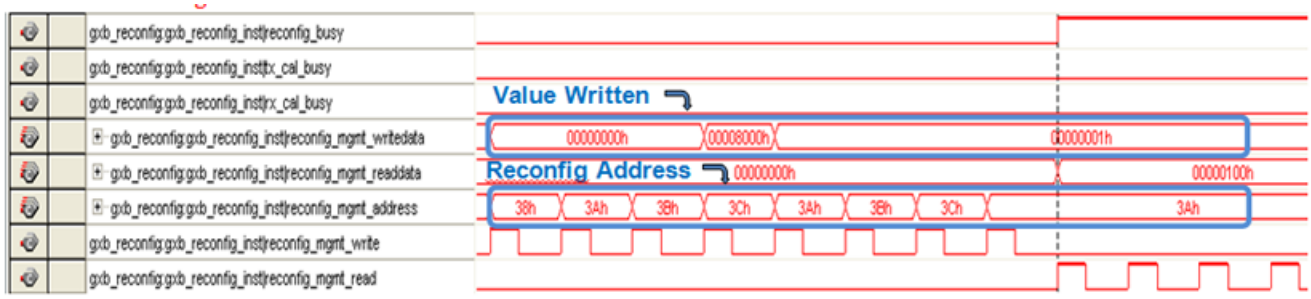
- *ch0_autoneg* - trigger reconfiguration process for CPRI Ch0
- *ch1_autoneg* - trigger reconfiguration process for CPRI Ch1

The CPRI channels will switch rate independently each time *ch0_autoneg* or *ch1_autoneg* is triggered. The rate switches in the following progression: 6144 Mbps > 4915.5 Mbps > 3072 Mbps > 2457.6 Mbps > 1228.8 Mbps and back to 6144 Mbps. To accomplished this, you are actually reconfiguring the TX local clock divider settings, CDR settings and performing a TX PLL switch.

Table 4: ISSP and Its Control in the Design Example

Bit	ISSP	Description
[2]	N/A	N/A
[1]	ch1_autoneg	Trigger reconfiguration process for ch1
[0]	ch0_autoneg	Trigger reconfiguration process for ch0

Figure 16: Signal Tap Results Showing the Streamer-based Reconfiguration Address and Data Written



Related Links

Refer to the Streamer section of the Altera Transceiver PHY IP Core User Guide for a description of the Streamer module.

Manual Trigger for DCD Calibration IP via the Register-based Reconfiguration Method

You need to trigger the DCD calibration IP when you are switching from 6144 Mbps to 4915.2 Mbps because it switches the clock network. These procedures describe how to trigger the DCD calibration IP manually.

Note: Arria V GZ and Stratix V devices do not require this DCD calibration.

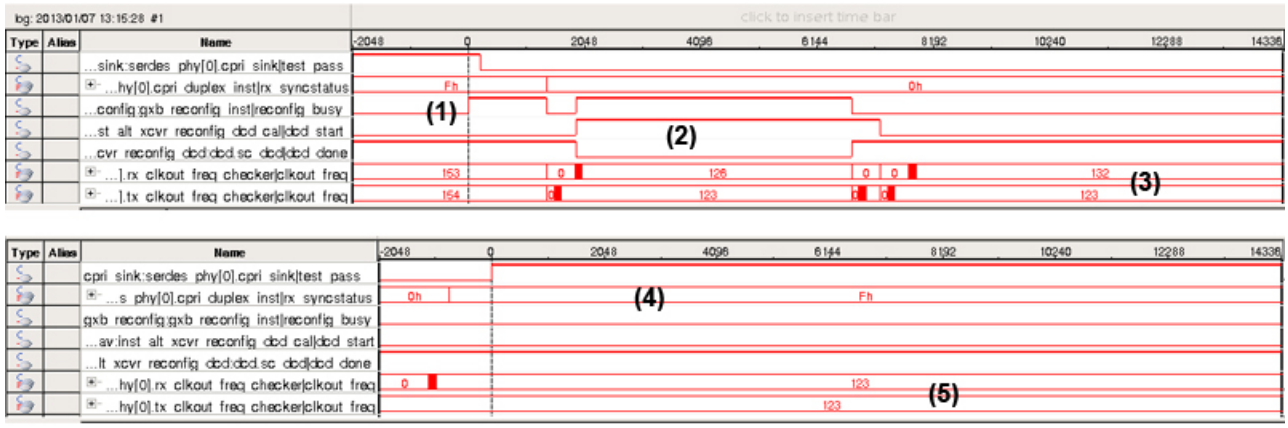
1. Specify the logical channel address at **0x48**.
2. Specify the data offset to DCD calibration mode at **0x4B** with data value **32'h0**.
3. Write to address **0x4C** with data value **32'h1**.
   Setting a '1' enables the DCD calibration IP.
4. Wait for `reconfig_busy` signal to deassert, indicating the completion of DCD Calibration process.
5. Write to address **0x4C** with data value **32'h0**.
   Setting a '0' disable the DCD calibration IP.

   Note: You should reset your channel after each manual DCD calibration.

Verifying Results in Signal Tap

Refer to `stp1.stp` files in the design for the hardware verification results.

Figure 17: STP Results Showing CPRI Channel Data Rate Switch and DCD Calibration Process



Notes:

1. The `reconfig_busy` signal is asserted high during the streamer-based reconfiguration process.
2. Manual trigger on DCD calibration. The `reconfig_busy` signal is asserted high. The `dcd_start` and `dcd_done` signals indicate the DCD calibration process.
3. The `rx_syncstatus` signal is deasserted during rate switch. The `tx_clkout` signal is updated with new frequency output.
4. After performing the PHY reset, the `rx_clkout` signal is updated and the `rx_syncstatus` signal is asserted as well. Eventually, the `test_pass` signal is high, indicating that the **cpri_sink** has verified correct data after the rate change.
5. The `tx_clkout` and `rx_clkout` signals are updated to the new frequency of 123 MHz (122.88 MHz) from 153.6 MHz after reconfiguration.

Duty Cycle Distortion Calibration

Duty Cycle Distortion (DCD) calibration is used to calibrate TX duty cycle due to the skew introduced by different clock networks.

In CPRI applications, when you are switching rate from 6144 Mbps to 4915.2 Mbps using two different TX PLLs you need to perform manual DCD calibration after the rate switch is completed. This is because the DCD calibration will compensate for the duty cycle distortion contributed by different clock networks during the TX PLL switch. The condition of triggering the manual DCD calibration IP in Arria V GX/GT and Cyclone V GT devices are:

- data rate is ≥ 4915.2 Mbps
- switching between clock networks (TX PLL Switching)

If both conditions are met, you need to trigger the manual DCD.

Note: DCD calibration process will kick-start once during power up if the data channel is running ≥ 4915.2 Mbps. You need to enable **Calibrate duty cycle during power up** in the Transceiver Calibration Function section in the Reconfiguration Controller IP as shown in *Figure 15*.

Summary

As demonstrated with the design example, the reconfiguration controller provides an easy and efficient method to dynamically change the functionality of Arria V deterministic latency PHY IPs to accommodate the need of CPRI rate change from 6144 Mbps down to 1228.8 Mbps.

Document Revision History

Table 5: Document Revision History

Date	Version	Changes
January 2013	2013.02.08	• Reorganized content and updated template.
December 2012	1.1	Updated Table 2
January 2012	1.0	Initial release