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Platform Brief

Accelerating AI and HPC with Advanced Process and Packaging Technologies

Intel Foundry offers a unique portfolio of process nodes, technologies, and packaging solutions to help AI and HPC silicon companies scale their performance.

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AI and HPC Demand High-Performance Silicon

The explosive growth of generative and agentic AI is driving record demand for powerful, energy-efficient computing solutions. This has transformed semiconductor manufacturing to chiplet-based architectures, enabling the modular assembly of dies based on different nodes from various vendors, thereby boosting performance and reducing costs. Simultaneously, supply chains are being restructured to enhance resilience, mitigate geopolitical risk, and promote sustainability.

Meeting these demands requires foundries to deliver advanced technologies, including leading-edge nodes for optimal performance per watt, robust multi-die interconnects, high-bandwidth memory (HBM) solutions, and efficient power delivery and thermal management for reliability. Supporting large, customizable multi-die systems provides designers with the flexibility and integration required for next-generation AI workloads.

Intel Foundry delivers a comprehensive portfolio of technologies that empower advanced AI and high-performance computing (HPC) designs, combining cutting-edge process nodes, high-performance packaging, and a broad intellectual property (IP) ecosystem.

Portfolio of Process Nodes for AI and HPC

Intel Foundry delivers a portfolio of advanced process nodes designed to meet the demanding performance, power, and area (PPA) targets of AI and HPC workloads. Starting with Intel 18A, these nodes integrate breakthrough technologies for compute density, power delivery, and performance.

Intel 18A

The Intel 18A family introduces **RibbonFET** Gate-all-around (GAA) transistors and **PowerVia** backside power delivery, offering significant performance improvements (see Figure 1).

These technologies enable higher transistor performance, improved electrostatic control, and reduced IR drop, critical for sustaining AI and HPC workloads under extreme power and thermal constraints.

All nodes in the Intel 18A family support high-performance (180H) and high-density (160H) standard cell libraries, which achieve over 30% density improvement compared to Intel 3.[1]

PowerVia frees up frontside routing for signals, enabling tighter layouts that reduce resistance-capacitance (RC) delay, while electronic design automation (EDA) tool support ensures seamless integration.

Intel 18A Delivers		
18% performance per watt increase (at same power) vs. Intel 3	1.3x chip density improvement vs. Intel 3	38% power reduction (at same performance) vs. Intel 3

Figure 1. Intel 18A delivers improvements in performance and power efficiency compared to Intel 3.[1]

RibbonFET

RibbonFET is Intel Foundry's first new transistor architecture since FinFET in 2011, introducing GAA with ribbon-shaped channels fully surrounded by the gate. This structure provides superior electrostatic control, enabling stable operation at lower voltages and reducing leakage—critical for power-constrained AI accelerators. A single ribbon stack delivers the same current as multiple FinFET fins in a smaller footprint, boosting density and supporting massive parallelism in compute arrays.

RibbonFET also improves short-channel control for high-speed logic and scales efficiently for future nodes.

PowerVia

PowerVia is the industry's first backside power delivery technology, now supported by EDA reference flows for Intel 18A designs. Relocating the power grid to the die's backside improves signal integrity and frees frontside metal for logic, enabling **an approximately 10x reduction** in worst-case dynamic voltage droop compared to frontside power.[2] For AI and HPC workloads, this architecture is critical for stabilizing operational voltage and minimizing timing violations during rapid, high-current transients that can reach hundreds of amps in large compute arrays.

Backside power frees up frontside routing resources, enabling shorter, cleaner signal paths and **improving routing closure by 8-10%**. In addition, this supports higher cell utilization and improved throughput.[2] The cost of adding a backside power delivery network is offset by streamlined lower metal patterning. Direct-print extreme ultraviolet (EUV) and relaxed signal pitch **reduce mask count by up to 44% and process steps by up to 42%** at the two lowest signal routing layers, lowering cost per wafer.[2]

Intel Foundry has partnered with EDA ecosystem vendors to optimize design flows for PowerVia, including improved routing engines, clock network shielding, buffer placement, and a reduction in buffer count.

RibbonFET + PowerVia Improves CPU Performance

CPU cores built with RibbonFET and PowerVia show a stronger frequency response as voltage increases. Production silicon data shows that these CPU cores deliver **~30% higher frequency at ~0.5V** compared to FinFET designs,[3] enabling more compute per watt for scaling and higher sustained throughput for demanding workloads.

Omni MIM

Omni MIM provides the industry's highest announced capacitance density (397 fF/μm²) for metal-insulator-metal capacitors, embedded in backside metals and adaptable for advanced packaging. This allows high-density decoupling on the chiplet, reducing inductance and improving transient response for AI and HPC systems. See "Spotlight on Power Delivery" for more on our power-delivery solution.

Intel 18A-P

Intel 18A-P extends the Intel 18A family with a performance-optimized, design-compatible variant, enabling additional headroom for HPC and AI systems. Built on the same RibbonFET and PowerVia innovations as Intel 18A, Intel 18A-P delivers measurable performance and power-efficiency gains in fully routed designs. These gains are driven by coordinated device, interconnect, and thermal enhancements. See Figure 3 for key improvement gains.

Intel 18A-P expands the RibbonFET device portfolio with a broader set of tunable options across both 180 HP and 160 HD cell libraries, enabling more precise power–performance optimization. As shown in Figure 2, **RibbonFET with Power Boost** (W3P) sits at the high-performance end of the device spectrum, extending beyond the W3 design point through improved mobility and a low-resistance dual contact architecture that combines frontside and direct backside contacts. This increases available drive current at matched capacitance, delivering **over a 10% frequency improvement on critical logic paths**. Complementary low-power (e.g., W1) and standard devices allow designers to apply peak performance selectively, maintaining overall power efficiency while targeting frequency-critical paths.[4]

Additional device and library enhancements improve design flexibility and timing control. New lower-threshold voltage (Vt) options for logic and **33% tighter skew corners**[4] enable more precise tuning across aggressive frequency targets and wide operating conditions. This improves timing closure and efficiency in large, heterogeneous compute designs.

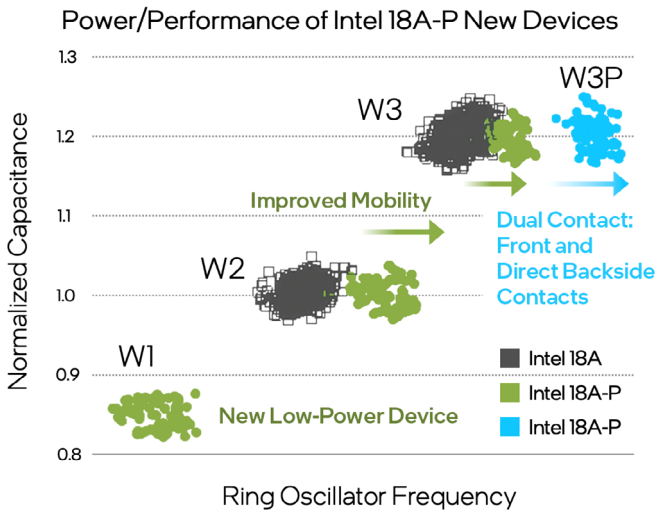

Figure 2. Updated 180 HP library devices. Power Boost offers a high-performance option within a broader, tunable set of devices.[4]

Improvements in lower metal interconnect resistance, combined with PowerVia's separation of power and signal routing, increase timing margin and routing efficiency under sustained load. Platform-level thermal improvements—including a **20-40% reduction in thermal resistance**[4]—help reduce temperature increase in high-power designs, supporting more consistent frequency scaling and sustained performance in large compute dies.

Intel 18A-P Delivers		
9% performance per watt increase (at same power) vs. Intel 18A	1x chip density vs. Intel 18A	18% power reduction (at same performance) vs. Intel 18A

Figure 3. Intel 18A-P delivers improvements in performance and power efficiency compared to Intel 18A, with full design rule compatibility.[4]

Intel 18A-PT for 3D Integration

Intel 18A-PT is the industry's **first announced base die with backside power delivery**, designed for next-generation 3D integrated circuit (3DIC) architectures, including high-bandwidth memory (HBM) applications (see Figure 4). Building on Intel 18A-P, it adds **pass-through and die-to-die through-silicon vias (TSVs)** along with hybrid bonding, enabling logic-stacking configurations to bring high-bandwidth memory closer to compute resources. This proximity reduces latency and increases memory density, critical for AI workloads that require rapid data access and large model storage.

Intel 18A-PT is Set to Deliver		
~9x die-to-die bandwidth density vs. Intel 3-T	20-25% chip density increase vs. Intel 3-T	25-35% power reduction vs. Intel 3-T

Figure 4. Intel 18A-PT improves bandwidth density, chip density, and power efficiency compared to Intel 3-T (Intel Foundry's base die derivative of Intel 3), offering a more capable base die for multi-chip packages.[5]

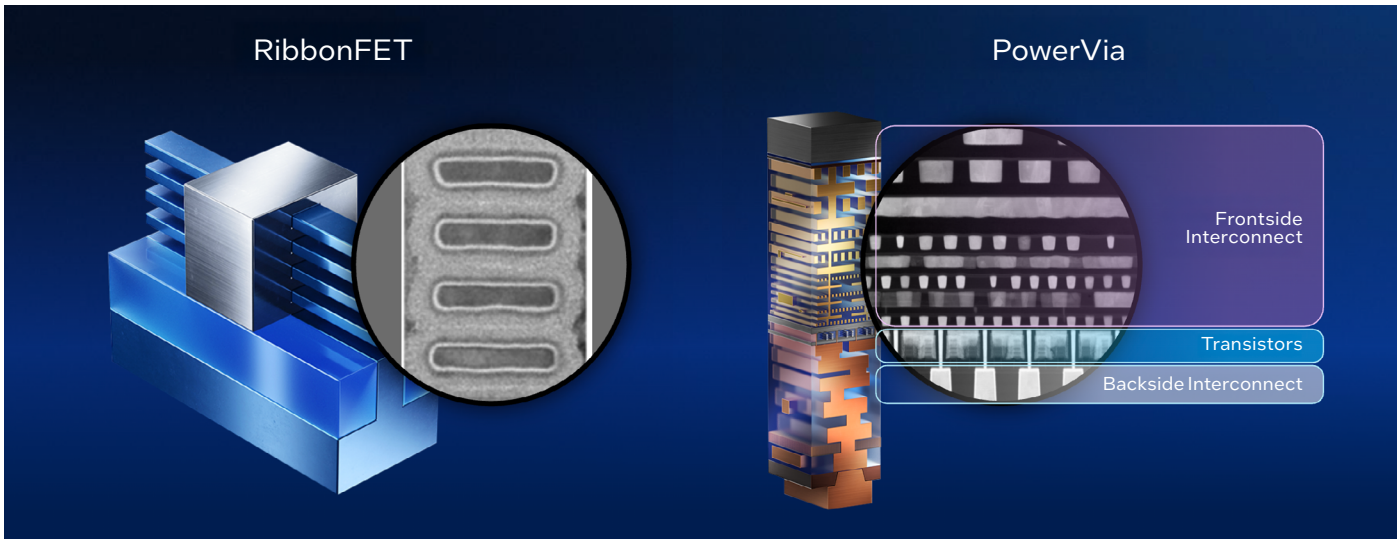

Figure 5. RibbonFET introduces Gate-all-around (GAA) transistors for improved control, higher drive current, and a smaller footprint. PowerVia delivers backside power delivery to enhance chip scaling, reduce IR drop, and simplify lower metal patterning.

Intel 14A

Building on Intel 18A, Intel 14A introduces **RibbonFET 2, the second generation of GAA transistors**, and **PowerDirect, an advanced backside power delivery technology**, delivering higher performance per watt and greater transistor density (see Figure 6).

Turbo Cells, specialized libraries for performance-critical paths, are a major innovation. Double-height Turbo Cells provide exceptional drive current in an area-efficient format, enabling higher CPU frequencies and GPU throughput with minimal power impact. Integrated into EDA flows, Turbo Cells enable designers to balance high-performance and power-efficient cells within compute-intensive blocks.

Intel 14A is Set to Deliver		
15-20% performance per watt increase (at the same power) vs. Intel 18A	1.3x chip density vs. Intel 18A	25-35% power reduction (at the same performance) vs. Intel 18A

Figure 6. Intel 14A improves performance, chip density, and power efficiency compared to Intel 18A.[6]

Design, Packaging, and Test Services for AI and HPC

As die sizes increase, AI and HPC developers require advanced packaging technologies to integrate high-density compute with memory that achieves high yields. Intel Foundry Advanced System Assembly and Test (Intel Foundry ASAT) leads in chiplet technology, offering end-to-end packaging and test solutions that improve yield and accelerate cycle times for complex multi-chip systems.

With over a decade of chiplet design and production experience, we enable flexible integration, mixing chiplets from any foundry to combine Intel dies with third-party components or deliver packaging-only services. For large, complex solutions, Embedded Multi-die Interconnect Bridge (EMIB) technology enhances die-to-die connectivity, enabling systems that exceed 8x the reticle size.

Our portfolio spans architectural optimization, layout, and analysis for cost, performance, and yield, plus test-only services for sorting and system-level validation.

We're advancing next-generation technologies, such as glass substrates and co-packaged optics, which promise transformative bandwidth and scalability for future AI and HPC systems.

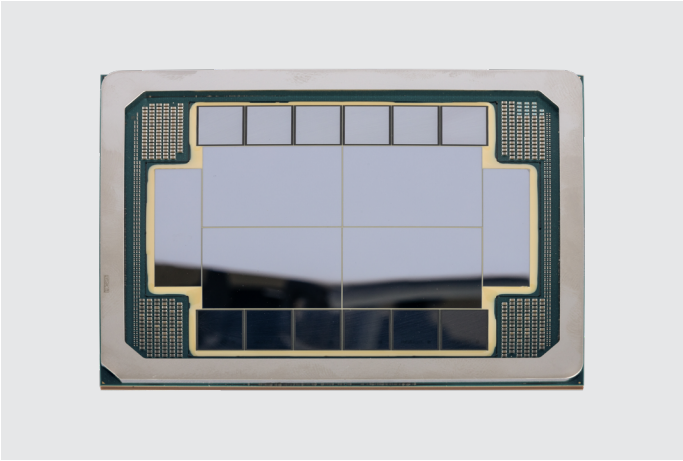

Figure 7. Image shows an AI chip test vehicle with an architecture that has high-bandwidth memory at the image top and bottom, high-speed communications at the left and right of the image, and GPU space in the middle. A test vehicle tests the manufacturing process but does not create a working product.

Embedded Multi-die Interconnect Bridge: EMIB 2.5D

Intel Foundry's unique EMIB 2.5D interconnect supports high-data-rate signaling between adjacent dies, utilizing simple driver/receiver circuitry to meet the high data throughput requirements of AI and HPC applications.

It embeds die-to-die bridges in the substrate, eliminating the need for and cost of an interposer and the associated wafer-level assembly stacking process. This cuts manufacturing time and eliminates any wafer-assembly yield loss with the ability to increase the area of the package.

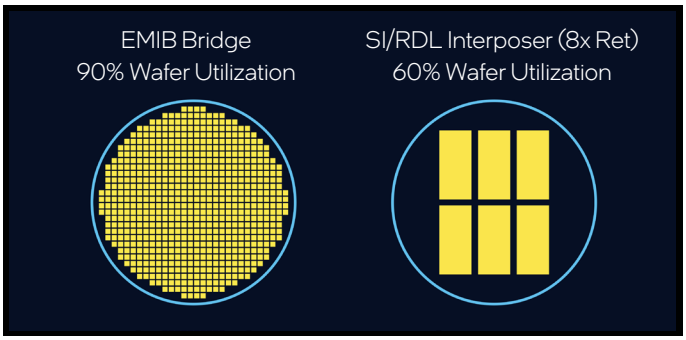

Figure 8. EMIB offers higher wafer utilization and yield compared to interposer architectures.

Our latest version, EMIB-T 2.5D, adds TSVs for stitching the die to HBM4 memory and ultra-high-speed Universal Chiplet Interconnect Express (UCIe) die-to-die communications. EMIB-T enables designs to be converted from other packaging technologies with minimal redesign. EMIB-T also allows vertical power delivery to minimize DC and AC noise.

EMIB-T 2.5D supports the growth of AI and HPC solutions with more than 8x reticle size in 2026 and 12x in 2028 (see Figure 9).

Year	Reticle Size	Package Size	HBMs	EMIBs
2023	~4x	~80x80	8	12
2026	> 8x	~120x120	12	> 20
2028	> 12x	> 120x180	> 24	> 38

Figure 9. EMIB-T delivers scalability now and in the future to support AI demand.

EMIB 3.5D and Foveros Direct 3D

EMIB 3.5D combines embedded bridges with vertical die-stacking to deliver high-performance and flexibility. Foveros 2.5D stacks chiplets on a passive base die, while Foveros Direct 3D stacks them on an active base die, increasing functionality. Foveros Direct 3D uses hybrid bonding interconnect, with sub-5µm copper-to-copper bump pitches, to ensure ultra-low-power, low-resistance connections.

Advanced Chiplet Test

As package sizes grow and complexity increases, comprehensive end-to-end testing is essential for quality and cost control. With final products often worth thousands, identifying known good dies is critical for maximizing yield. The Intel Foundry singulated die sort test accelerates the identification of known good dies. Our advanced methodology uses active thermal controls for precise, consistent testing.

Additionally, our system-level testing (SLT) detects marginal chip defects missed by traditional methods. SLT simulates real-world scenarios to uncover issues that only appear under actual operating conditions.

Our end-to-end testing solutions are optimized for our proprietary High Density Modular Test (HDMT) equipment. We also offer testing on commercial automated testing equipment (ATE) to meet your needs. With these solutions, Intel Foundry delivers reliable, high-quality products.

Spotlight on Power Delivery

Generative and agentic AI workloads exert intense power demands on multi-die systems, causing rapid current surges at microsecond and nanosecond timescales that can destabilize conventional power delivery networks.

Intel Foundry solves these challenges with a holistic stack of innovations, beginning at the transistor level. Intel 18A logic tiles feature PowerVia backside power delivery, which dramatically shortens the power path, reduces IR drop, and frees up frontside routing for high-speed signaling. Paired with on-die Omni MIM capacitors, this architecture minimizes inductive droop during fast transients, helping to maintain frequency during bursty AI loads. Omni MIM capacitors also shrink power delivery network (PDN) impedance at high frequencies.

At the package level, EMIB-T 2.5D incorporates TSVs and high-power MIM capacitors directly in the bridge, eliminating cantilevered power traces and enabling vertical power delivery with lower impedance and improved reliability. These improvements are essential for meeting the increased bandwidth requirements of HBM4 and future generations, as well as UCIe operating at speeds of 32 Gbps and higher.

To further stabilize power delivery, Intel Foundry integrates embedded deep trench capacitors (eDTC) for ultra-high capacitance density close to the load, thereby flattening PDN impedance across the base die. Embedded MIM (eMIM-T) technology delivers superior decoupling at the base die, leveraging the same advanced architecture as Omni MIM, even on mature nodes. For precise, high-speed point-of-load regulation, CoaxMIL technology embeds magnetic inductors into the substrate, enabling integrated voltage regulators (IVRs) with rapid response and minimal loss.

Together, these technologies form a scalable power delivery fabric that keeps pace with rising compute density.

eMIM-T
> 2.5 µF/mm²

CoaxMIL
2.5-5.0 nF/mm²
> 10 A/mm²

eDTC
> 2.5 µF/mm²

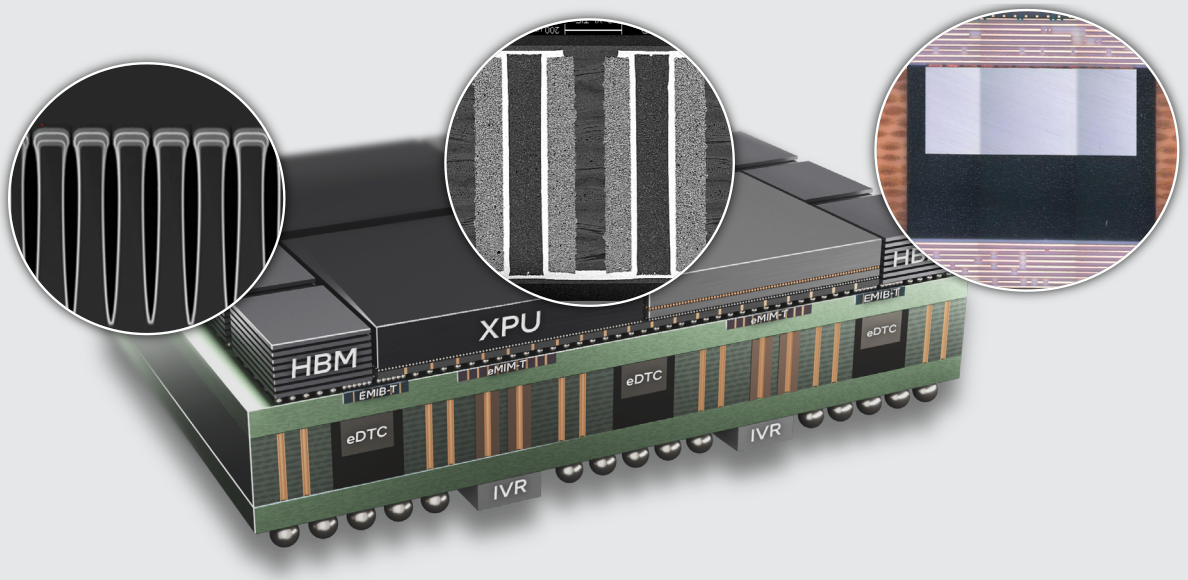

Figure 10. An example of the Intel Foundry power delivery solution shown at Intel Direct Connect 2025, this image showcases the forward-looking plans for increased eMIM-T capacity. All product plans and roadmaps are subject to change.

Tap into the Intel Foundry Ecosystem

The Intel Foundry Accelerator Alliance helps customers turn their innovations into silicon by leveraging the world-class capabilities of partners from across the design ecosystem, including IP, proven tools and flows, cloud capabilities, and design acceleration services.

Recent alliance expansions add collaboration for chiplet interoperability and streamlined spec-to-silicon delivery, potentially accelerating complex application time to market. These efforts complement co-optimization initiatives that align process and system technologies with workload-specific needs.

To meet the demands for high-bandwidth, low-latency, die-to-die communication from AI and HPC, Intel Foundry supports **UCIe 1.1 and 2.0**, the open standards for chiplet interconnect. UCIe ensures interoperability across foundries, reduces integration cost, and speeds deployment. UCIe 2.0 introduces optical interconnect and advanced packaging support, enabling modular and scalable architectures for next-generation AI and HPC systems.

Transform Your Silicon Vision into Reality with Intel Foundry

Intel Foundry offers full-stack solutions that accelerate time to market, energizing the industry transition from "system on chip" to "system of chips." Our integrated approach combines cutting-edge process node technologies—from mature nodes to leading-edge processes—with revolutionary advanced packaging solutions and select systems technologies.

Ready to revolutionize your next-generation products? Visit intel.com/foundry.

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[1] K. Fischer et al., "Intel 18A Platform Technology Featuring RibbonFET (GAA) and PowerVia for Advanced High-Performance Computing," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2025.

[2] E. Karl et al., "Backside Power: Enabling Energy-Efficient Performance on Advanced Node Designs," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2026.

[3] M. Shamanna et al., "CPU Cores in GAA with Backside Power: Silicon-Validated Design Insights," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2026.

[4] A. Bowonder et al., "Intel 18A-P CMOS Technology Enhancement Featuring Advanced RibbonFET (GAA) Transistors and PowerVia for High-Performance Computing," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2026.

[5] Based on Intel internal analysis comparing Intel 18A-PT to Intel 3-T as of April 2025. Results may vary.

[6] Based on Intel internal analysis comparing Intel 14A to Intel 18A as of April 2025. Results may vary.

Performance varies by use, configuration, and other factors. Results may vary.

All product and service plans, roadmaps, and performance estimates are subject to change without notice. Projections about future node performance and other metrics are inherently uncertain. Performance results are based on testing as of dates shown. Your costs and results may vary.

This document contains forward-looking statements about Intel's future plans or expectations, including its process and packaging technology roadmaps. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

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