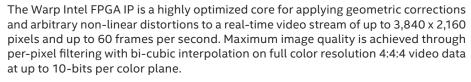


Warp Intel® FPGA IP

The Warp Intel® FPGA IP is a highly optimized IP core for applying geometric corrections and arbitrary non-linear distortions to a real-time video stream.







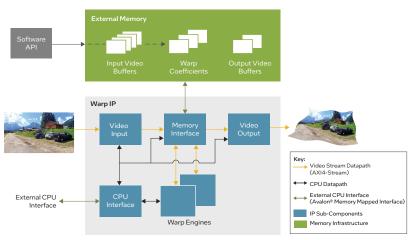












The Warp Intel FPGA IP is delivered with a set of software components including a software driver that configures and controls all the necessary parameters of the IP, a warp data generator, and an example warp mesh generator. The software can be deployed on a Nios® II processor-based system or SoC (recommended).

Applications

Warp distortion and correction IP can be used in a range of applications including:

- Video projectors from cinematic and simulators to consumer/short-throw - for lens and curved screen compensation
- · 2D and stereo 3D Image capture, alignment, registration and projection
- Camera lens distortion and chromatic aberration correction
- · Virtual reality headsets
- · Multi-camera image stitching
- · Manipulation and registration of overlays, HUDs interactive graphical and web content

Standard and Arbitrary Transforms

The Warp Intel FPGA IP allows the input image to be transformed using a number of controls to perform:

- Fish-eye, barrel and general lens/screen correction
- · Keystone and pin-cushion correction
- · Resizing and rotation
- · Perspective mapping
- · Arbitrary warps up to local expansion/compression limit

The Warp Scaler block manipulates the image either using high-level instructions such as rotate, keystone, barrel or a mesh mapping from the warp load direct memory access (DMA) block. The input image is stored and manipulated in external SDRAM via the Avalon® Memory-Mapped interconnect.

Key Features

- · Arbitrary warp transforms and rotations
- · Highly optimised external memory interface
- 0.5x to 2x local scaling
- · High quality per-pixel bi-cubic interpolation
- · Coefficient sets available for highest filter quality
- Full data buffering to allow input and output to operate on independent clock domains
- Support for 10 bit per color component
- Support up to 2 pixels in parallel per clock processing
- Low latency
- Support resolutions up to 3840 × 2160 at 60 fps and future support for up to 8K at 60 fps
- · Low FPGA resource utilisation
- AXI4-Stream video I/O interface
- AXI4-Stream ↔ Avalon-Stream Protocol Converters
- Avalon® Memory-Mapped CPU control and memory interfaces

Customer Benefits

- Low resource yielding lower power 'Edge' implementations
- · Continuous 360-degree rotations
- · Continuous scaling factors
- Free Intel® FPGA IP Evaluation Mode
- Design example available in Intel Resource and Design Center
- Avalon® or AXI interfaces
- Fully maintained and supported by Intel

Supported Devices

- Intel® Cyclone® 10 GX FPGA
- Intel[®] Arria[®] 10 FPGA
- Intel® Stratix® 10 FPGA
- Intel Agilex® FPGA

Design Your Product Today with Intel FPGAs

Intel provides a large range of complementary and modular IP cores for video processing and connectivity. These IP cores can be used to create complete solutions for applications in Studio Broadcast, ProAV, Aerospace/Defense, Medical, Consumer, Automotive, Machine Vision, and more.

More information is available about Intel video IP at www.intel. com/content/www/us/en/broadcast/products/programmable/overview.html or contact an Intel sales representative.

Design Example

Intel® Arria® 10 GX FPGA Development Kit. Fully compatible with Intel IP cores.

Typical Resource Use

Device	ALMs	M20K	DSPs
Intel Agilex FPGA	6,871	73	54
Intel Arria 10 FPGA	9,468	97	99

Useful Links

- Intel FPGA Warp IP Design Example Requires Intel Resource & Design Center access
- Intel® Arria® 10 GX FPGA Development Kit
- Intel® Cyclone® 10 GX FPGA Development Kit
- Intel® Stratix® 10 GX FPGA Development Kit
- Intel Agilex® 7 FPGA Development Kit



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