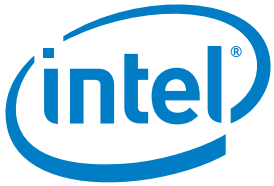

Intel® Enpirion® Power Solutions

Using the Gen5 VRTT to Validate Intel® Stratix® 10 MX FPGA Voltage Regulators

Application Note

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1. Introduction

Intel has designed hardware validation tools such as the Voltage Regulator Test Tool (VRTT) to characterize power supply robustness for many years now. In the past, these VRTTs were solely limited to validating the power supply of a CPU motherboard's core rail and were only of interest to the vendors who designed CPU core power themselves. With the addition of field programmable gate arrays (FPGAs) to Intel's vast portfolio, validation efforts have been expanded and we now have the capability to simply and quickly test multiple voltage rails on several FPGAs using the VRTT to enable designs to get to market much faster. In this app note, we will use the Gen5 VRTT to test the static and dynamic current of an Intel® Enpirion® EM2260P01QI PowerSoC to power the core of an Intel Stratix® 10 MX FPGA development kit.

The EM2260 is a fully integrated 60 A synchronous dual-phase buck converter digital PowerSoC that requires minimal external components to meet the core power specifications of an FPGA. It features an advanced digital controller, gate drivers, synchronous MOSFETs, and high-performance inductors. For added design flexibility and higher current capability, a footprint-compatible 80 A PowerSoC, EM2280P01QI, is also readily available.

2. Test Setup and Tools

Test Setup

The test setup is fairly simple and is shown in Figure 1. It would require an assembled prototype board (i.e. system under test), a Gen5 compatible interposer, male-to-male header, and the Gen5 VRTT. The only modification that would be necessary on your prototype would be to solder the interposer in place of the FPGA so that the Gen5 VRTT can be plugged in using the male-to-male header. A computer or laptop is also necessary to run the VRTT software to configure and read back the settings and test data for your system. In some cases you may need additional height clearance on your prototype board to plug in the VRTT and in those situations an additional riser board can be added to give you that extra height clearance.

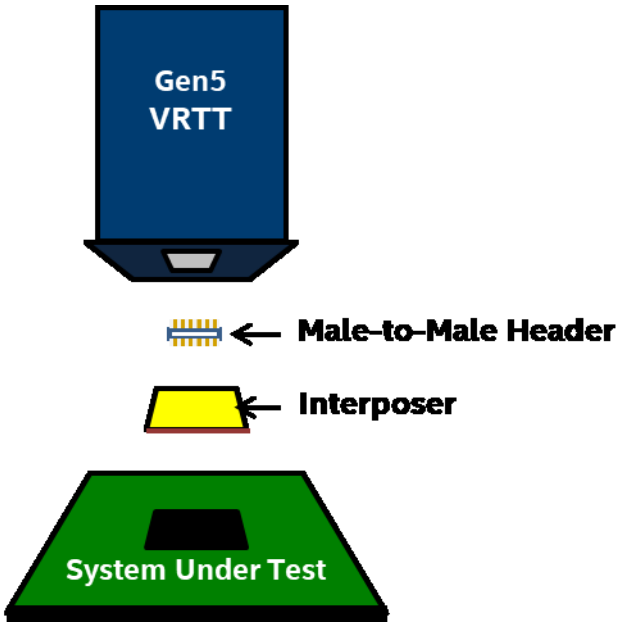

Figure 1: Test Setup Diagram

Gen5 VRTT

Intel's Gen5 VRTT shown in Figure 2 is a robust and flexible electronic loading tool that is capable of controlling and measuring the loads that would normally be applied by an FPGA in a system under test. The VRTT has eight individual load channels that are capable of up to 100 A each that are automatically partitioned once plugged into an interposer. The Gen5 VRTT includes companion software with a simple interface that incorporates a built in oscilloscope for measurement functionality and also has scripting capabilities. With the software, you can quickly run static and dynamic load testing of multiple simultaneous FPGA power rails to quickly validate power in your system. The VRTT inludes the necessary male-to-male header for mating with a compatible interposer and optional attachments are available to enable efficiency testing capabilities as well. The Gen5 VRTT can be purchased online at https://designintools.intel.com/.

Figure 2: Intel's Gen5 VRTT

FBGA2597-S10-F53 Interposer

As mentioned in the test setup, a Gen5 compatible interposer is necessary to be able to use the VRTT and must be soldered in place of the FPGA on your system under test. The interposer is a female socket that mates to the VRTT via a male-to-male header. Once the VRTT is plugged in and powered on, the VRTT will detect the specific interposer it is plugged into, in this case the FBGA2597-S10-F53 for an Intel Stratix 10 MX FPGA shown in Figure 3, and automatically partition and group each of its channels to mimic the loads of your system's FPGA. It will allocate enough channels to cover the maximum loads for the core, transceiver, and other FPGA specific loads. The load allocation for the FBGA2597-S10-F53 interposer is shown in Table 1. The FBGA2597-S10-F53 interposer can be purchased online at https://designintools.intel.com/.

Figure 3: Gen5 Compatible Intel® Stratix® 10 MX FPGA Interposer

FPGA Rail	FBGA2597-S10-F53 Max Load Current (A)
VCC	300
VCCRL	12
VCCRR	12
VCCTL	12
VCCERAM	12
VCCIO_UIB	20

Table 1: FBGA2597-S10-F53 Interposer Current Allocation

3. Testing and Results

Testing the Intel Enpirion EM2260P01QI PowerSoC to Power the Core of the Intel Stratix 10 MX FPGA

Once all of the hardware is properly connected and powered up, you can then run the Gen5 software GUI. The GUI contains all the controls to select between different test modes, choose which power rail to test, toggle current controls, view the oscilloscope waveforms, and select necessary measurements.

The Intel Stratix 10 MX FPGA is a SmartVID graded device that requires the use of a configurable voltage regulator through the Power Management Bus (PMBus*) for proper performance. On our development kit under test we chose to use a c-capable Intel Enpirion 60 A power module with integrated inductor, the EM2260P01QI. We chose this device because it can easily meet the static and dynamic voltage specifications of the Intel Stratix 10 FPGA and it comes in a small form factor for the amount of current it can provide.

To test the EM2260 to meet the Intel Stratix 10 MX FPGA's static voltage tolerance, you will first need to select "**VCC**" under the **Rail** drop down box in the upper right side of the GUI. Then you will need to select "**Static VID Static Current (SVSC)**" from the **Select Test Mode** drop down box. Once the rail and test mode are selected, you will then need to enable the oscilloscope by selecting **VCC** from the scope's drop down menu in the upper left portion of the GUI and then check the **CH1(A)** and **CH2(V)** checkboxes to display voltage and current. Finally to display measurements, you will need to click on the **Scope** menu and choose which measurements you'd like to have displayed, we have chosen **Min/Max** to verify that our voltage is within the specified tolerance window. After all GUI configurations are set, for the actual static voltage test we need to set the **ICC Static** slider to the maximum aniticpated DC current, 60 A. We then click the **Generate Wave** button to enable the load and observe our results below in Figure 4. The initial VCC output voltage is set to 0.9 V and has an allowable tolerance of +/-30 mV. From Figure 4 below, we can see that the min/max voltage is well within the +/-30 mV tolerance window at full load.

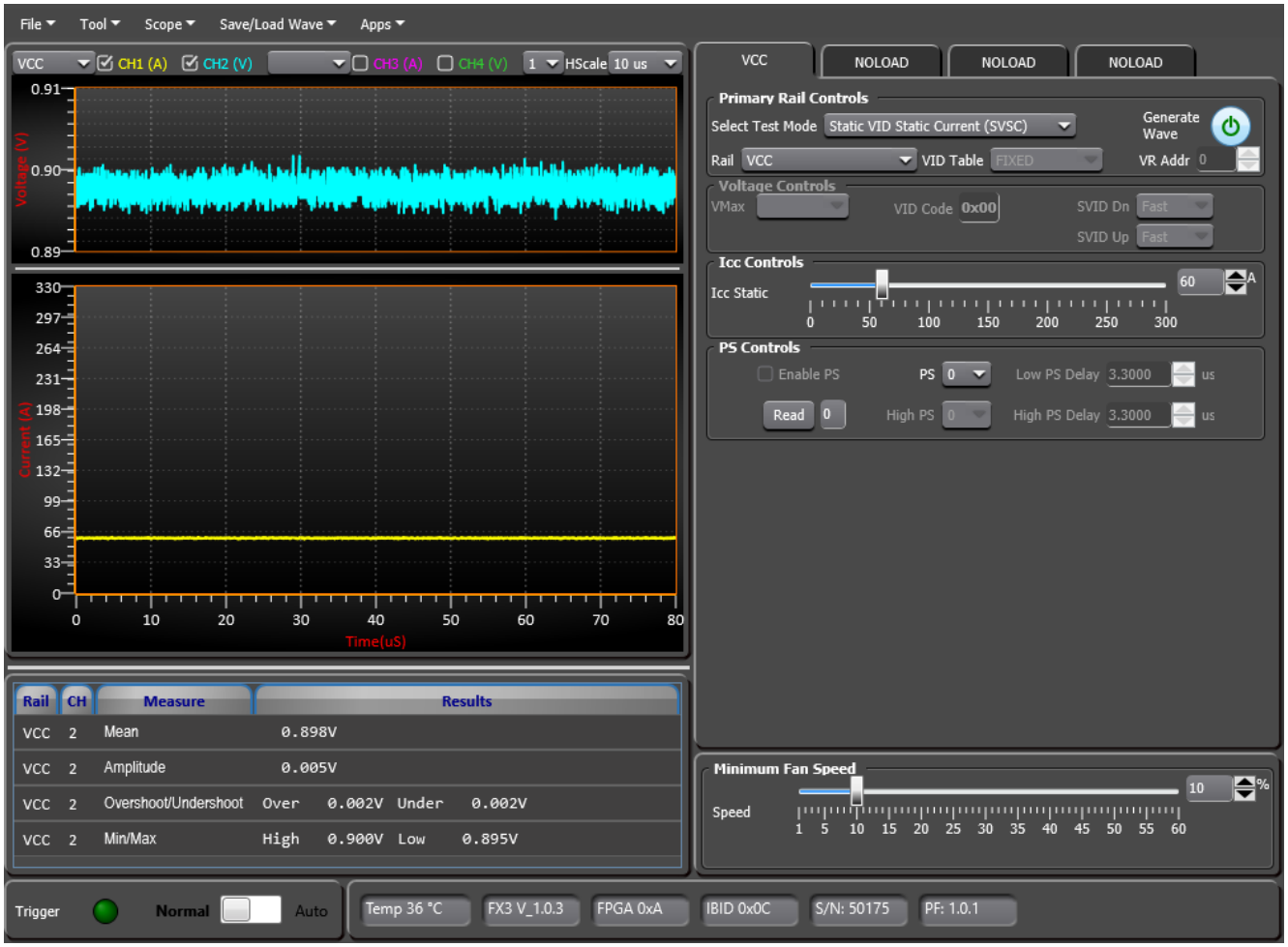

Figure 4: Static Testing on EM2260 for Core Rail (I_{OUT} = 60 A)

To test the EM2260 to meet the Intel Stratix 10 MX FPGA's dynamic voltage tolerance, you will first need to select "**VCC**" under the **Rail** drop down box in the upper right side of the GUI. Then you will need to select "**Static VID Dynamic Current (SVDC)**" from the **Select Test Mode** drop down box. Once the rail and test mode are selected, you will then need to enable the oscilloscope by selecting **VCC** from the scope's drop down menu in the upper left portion of the GUI and then check the **CH1(A)** and **CH2(V)** checkboxes to display voltage and current. Finally to display measurements, you will need to click on the **Scope** menu and choose which measurements you'd like to have displayed, we have chosen **Min/Max** to verify that our voltage is within the specified tolerance window. After all GUI configurations are set, for the actual dynamic voltage test we need to apply a 50% load step to VCC. To do this, the GUI will be configured as follows:

Icc Max: 30 A

Icc Min: 0 A

Frequency: 1 kHz

Duty Cycle: 50%

Ramp Time: 3,000 ns (10 A/us ramp rate)

We then click the **Generate Wave** button to enable the load and observe our results below in Figure 5. The initial VCC output voltage is set to 0.9 V and has an allowable tolerance of 5% or +/- 45 mV. From Figure 5 below, we can see that the overshoot/undershoot voltage is well within the +/- 45 mV tolerance window at full load.

Figure 5: Dynamic Testing on EM2260 for Core Rail (I_{OUT} Load Step = 0-30 A)

Other FPGA Voltage Rail Test Capabilities

In addition to the core rail, the Gen5 VRTT is capable of testing several other voltage rails of the Intel Stratix 10 MX FPGA. The other rails that are configured for test are VCCR, VCCT, VCCERAM, and VCCIO_UIB. Future capabilities may also be added to test the SmartVID functionality of the VCC core rail.

Other Test Tools Interposers Available

There are several other interposers available to test different package types of both Intel Stratix 10 FPGAs and Intel Arria® 10 SoCs. Some of these interposers are compatible with the Gen4 low power VRTT (LPVRTT) and it is important to keep in mind that you must use the correct test tool with the correct interposer (LPVRTT to LPVRTT interpose, Gen5 VRTT to Gen5 interposer, etc), they are not all interchangeable. Listed in Table 2 is a guide of all available interposers, their mating test tool, and the voltage rails/currents they support.

Interposer	**FBGA2397-S**	**FBGA1760-F43**	**FBGA1517**
FPGA	Intel® Stratix® 10 F50	Intel Stratix 10 F43	Intel Arria® 10 SoC F40
VCC	110	110	40
VCCR	20	17.5	10
VCCT	20	8.5	10
VCCERAM	10	11	5
VCCPT	x	11	10
VCCL_HPS	x	x	5
VCCIO2J	x	x	5
VCCIO2K	x	x	5
VCCIO3A	x	x	5
VCCIO3B	x	x	5
VCCIO3C	x	x	5
VCCIO3D	x	x	5
VCCIO3F	x	x	5
VCCIO_UIB	x	x	x

Table 2: Intel® Stratix® 10 FPGA and Intel Arria® 10 SoC Available Interposers + Mating Test Tools

Interposer	**BGA896**
Test Tool Version	Low Power VRTT
FPGA	Cyclone® V F31
VCC1P1_HPS-1.1V_HPS	2
VCCINT_FPGA-1.1V_FPGA	11.4
VCC2P5-2.5V_HPS	3
VCC_AUX	2
VCC3P3-3.3V_HPS	9
VCCIO3A	2
VCCIO5A	2
VCCPGM	2
VCC1P5_DDR3-1.5V_HPS	4
HSMC_VCCIO	1
HSMC_VCCPD	0.5
2.5V_FPGA	3.8
1.5V_FPGA	3

Table 3: Cyclone® V SoC Available Interposers + Mating Test Tools

4. Conclusion

We have introduced the Gen5 VRTT with interposer and applied it's capabilities to quickly test the static and dynamic conditions of an Intel Enpirion EM2260P01QI PowerSoC to power the core of a Intel Stratix 10 MX FPGA development kit. The Gen5 VRTT is a useful tool that can help expedite power validation on your system under test and help reduce your evaluation time and hence get you to market faster.

Revision	Description	Revision Date
P1	First Draft	8/21/2018
P2	Final Draft	5/30/2019