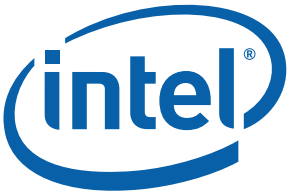

Intel® C620 Series Chipset

Boundary Scan Description Language (BSDL)

July 2017

Document Number: 336070-001US

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Revision History

Document Number	Revision Number	Description	Date
336070	001	• Initial Release	September 2016

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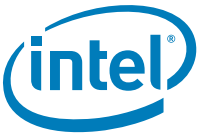


1 Introduction

1.1 About This Manual

This document will be used as a support document for the Intel® C620 Series Chipset Chipset Boundary Scan Description Language (BSDL).

This document is intended for the development of IEEE* 1149.6 Boundary scan tests for Intel® C620 Series Chipset products. This manual assumes a working knowledge of IEEE 1149.6 methodologies and the In Circuit Test (ICT) manufacturing test methods.

Chapter 1, “Introduction” - Provides information on the organization of this document.

Chapter 2, “PCH JTAG/Boundary Scan Test Mode” - Provides a detailed discussion of the implementation and use of the Boundary Scan Test mode via the JTAG interface in the PCH.

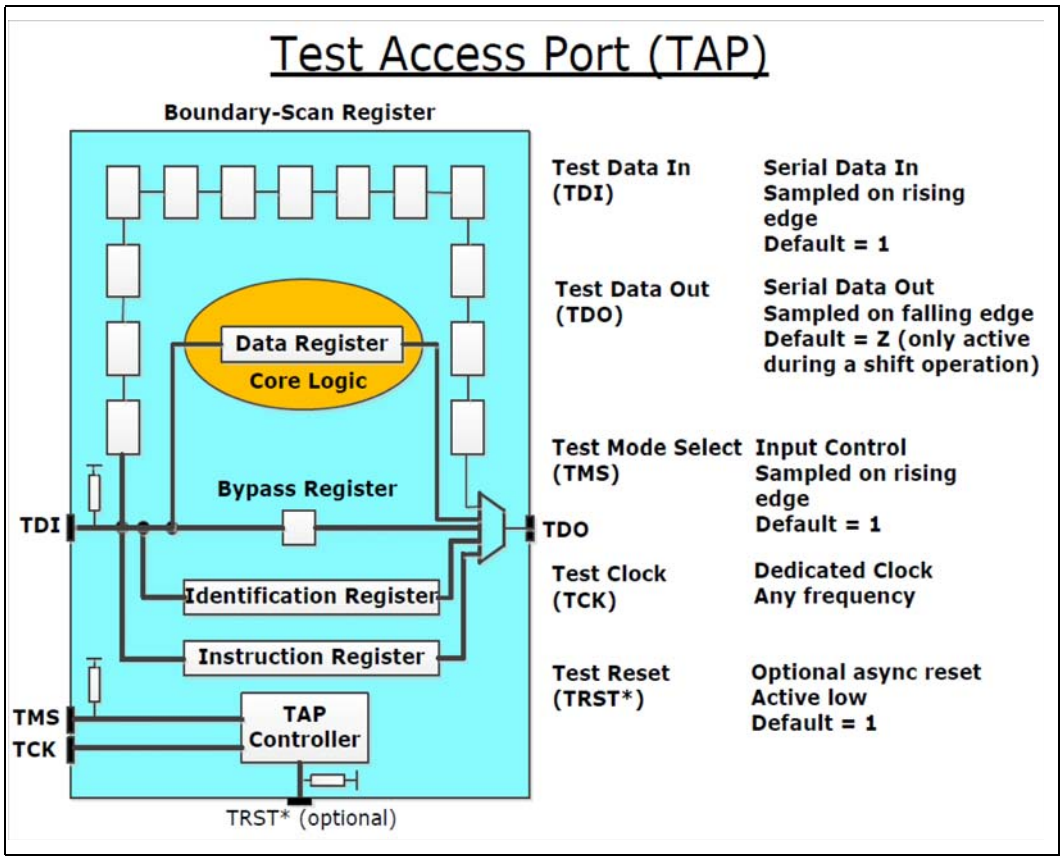
Note: This document applies to all Intel® C620 Series Chipset SKUs.

2 PCH JTAG/Boundary Scan Test Mode

2.1 TAP Controller

The Intel® C620 Series Chipset has dedicated JTAG pins and a TAP controller as shown in Figure 2-0. For detailed information on functionality of the interface, refer to these specifications: *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1-2001 Specification* and *1149.6-IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks – Specification*.

Figure 2-1. Tap Controller



In order to support boundary scan for AC coupled, high-speed I/Os, the master TAP supports IEEE 1149.6. This includes the extra instructions extest_pulse and extest_train. There is also an additional instruction that is not in the IEEE 1149.6 specification, defined by Intel, extest_toggle. For details on supported boundary scan instructions, refer to Table 2-0. The Intel® C620 Series Chipset network is accessed serially through four dedicated component pins as shown in Table 2-0.

Note: The 1149.1 specification also defines an optional TRST# TAP input pin, to asynchronously reset the TAP controllers. However, the Intel® C620 Series Chipset

does not implement this pin. Instead, each TAP controller is asynchronously reset by an internal power OK signal corresponding to the power well that it is in.

Table 2-1. JTAG Signals

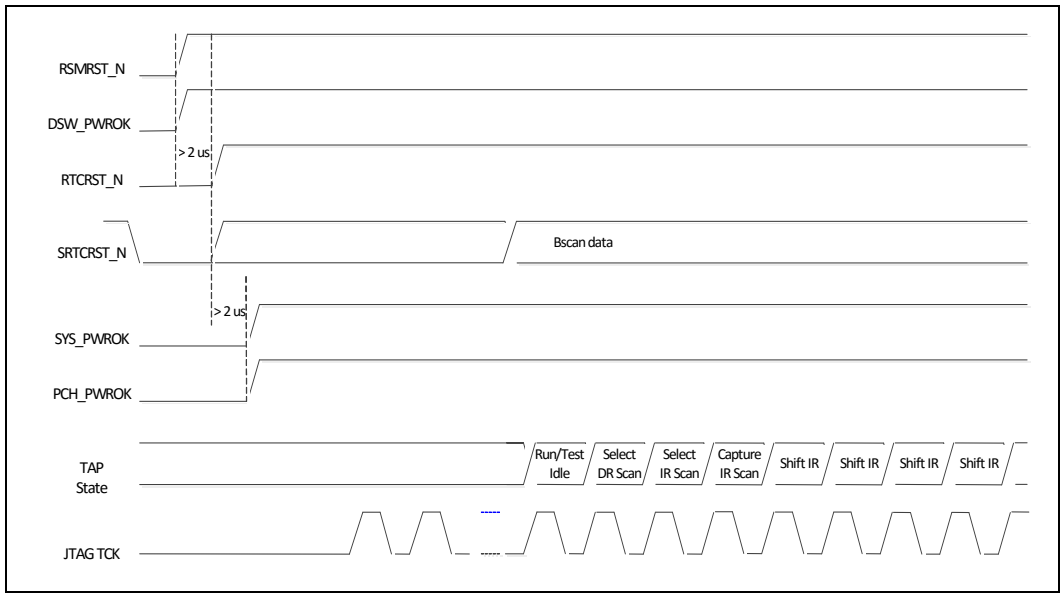
Name	Type	Description
JTAG_TCK	I/O	Test Clock Input (TCK): The test clock input provides the clock for the JTAG test logic.
JTAG_TMS	I/O	**Test Mode Select (TMS):** This signal is decoded by the Test Access Port (TAP) controller to control the test operation.
JTAG_TDI	I/O	**Test Data Input (TDI):** Serial test data and instructions are received by the test logic at TDI.
JTAG_TDO	I/O	**Test Data Output (TDO):** TDO is the serial output of the test instruction and data from the test logic defined in this standard.

During boundary scan test mode, the boundary scan unit will take over the I/O/AFE control for direct control to execute all the different IEEE 1149.1 and 1149.6 instructions.

2.2 JTAG Test Entry Mode

For functionality of the JTAG boundary scan interface, refer to the specification mentioned above. In order to enter the boundary scan test mode, multiple signals must be conditioned correctly. The test mode entry sequence is outlined in Figure 2-0 and the text that follows.

Figure 2-2. Boundary Scan Test Mode Entry



Signal Details:

- RSMRST_N is a hard reset to indicate the suswell is valid.
- DSW_PWROK is a hard reset to indicate the dswwell is valid.
- RTCRST_N is a hard reset to indicate the rtcwell is valid.
- PCH_PWROK is a hard reset to indicate the corewell is valid.
- SYS_PWROK is a hard reset to indicate the system has been power up.
- SRTCRST_N is a hard strap to enable bscan.

Power-Up Sequence:

- RSMRST_N and DSW_PWROK need to be driven from 0 to 1.
- Followed by RTCRST_N driven from 0 to 1 (~2 µs later or more).
- Followed by PCH_PWROK, and SYS_PWROK driven from 0 to 1 (~2 µs later).

Test Mode Entry Requirements:

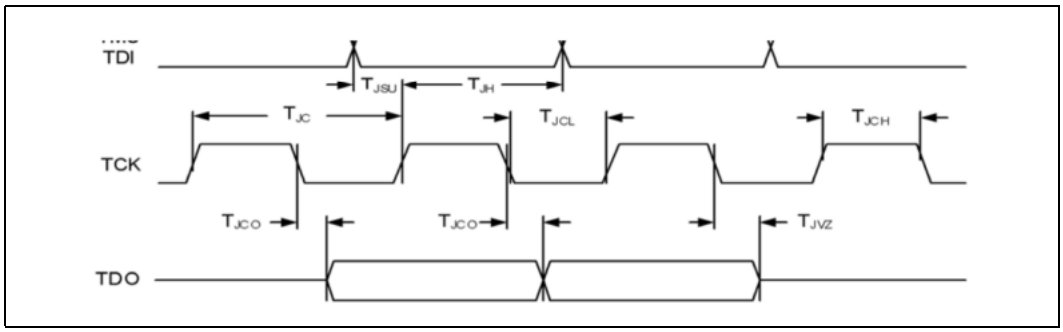
- SRTCRST_N is a reset and isolation override hard strap. This hard strap enables the boundary scan when driven to 0 when DSW_PWROK is 1. This is needed primarily if on-board clocks are not running. SRTCRST_N can be released after the RTCRST_N transition from 0->1 if not connected to RTCRST_N.
- SRTCRST_N is latched on the rising edge of DSW_PWROK.

Supported TCK Frequencies:

- The supported maximum frequency of TCK will be 2 MHz. A delay will be observed on the response of TDO with regard to the falling edge of TCK.

2.3 TAP Timing

Figure 2-3. JTAG Mode Initialization Cycles



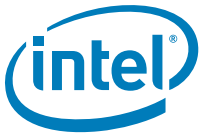


Table 2-2. JTAG Signal Timings

Symbol	Parameter	Min.	Max.	Unit	Notes
T_{JC}	JTAG TCK clock period	25		ns	40 MHZ
T_{JCL}	JTAG TCK clock low time	0.4 * T_{JC}		ns	
T_{JCH}	JTAG TCK clock high time	0.4 * T_{JC}		ns	
T_{JSU}	Setup of TMS and TDI before TCK rising	11		ns	
T_{JH}	TMS and TDI hold after TCK rising	5		ns	
T_{JCO}	TCK failing to TDO output valid		7	ns	
T_{JVZ}	TCK failing to TDO output high-impedance		9	ns	

2.4 Supported Instructions

The JTAG instruction register has predefined decodes for EXTEST (all 0s) and BYPASS (all 1s). The SAMPLE and PRELOAD are required instructions, but the decode value are user defined. The Intel® C610 series chipset implements the commands listed in Figure 2-0 in the TAP controller.

Table 2-3. JTAG Instruction Register Description

IR Opcode (9 Bits)	Rd/Wr Opcode (Bit[8])	Unique Opcode (Bit[7:0])	Command/Register (Length)
001h	0b	00h	SAMPLE/PRELOAD
002h	0b	02h	IDCODE(32)
004h	0b	04h	CLAMP
008h	0b	08h	HIGHZ
009h	0b	09h	EXTEST
00Dh	0b	0Dh	EXTEST_TOGGLE
00Eh	0b	0Eh	EXTEST_PULSE
00Fh	0b	0Fh	EXTEST_TRAIN
0FFh	1b	FFh	BYPASS

2.4.1 JTAG Instruction Registers

The following sections describe the registers shown in Table 2-0 in greater detail. Bit 8 is used as read/write bit for most registers, the corresponding aliasing address are implied unless specifically mentioned.

Note: The number of bits "N" depends on the number of boundary scan cells implemented.

2.4.1.1 Offset 01h: SAMPLE/PRELOAD - SAMPLE/PRELOAD for Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**SAMPLE:** Command for Boundary Scan. Select the Boundary Scan register and put the boundary scan cell in functional mode. Used to capture the functional signal connect to the boundary scan cell input.

2.4.1.2 Offset 02h: IDCODE - Identify Code for Boundary Scan

Bit	Type	Reset	Description
31:28	RO	0	**Version:** Used to identify the variant of the component type. Implementation Note: Implement to make the value change in any metal layers.
27:12	RO	A113h	**Part Number:** Unique value to represent the component. Intel® C620 Series Chipset part number is A114h.
11:1		00000 00100 1b	**Manufacture Identity:** Intel identity is 00000001001b.
0	RO	1b	**Hard code to 1** as indication of start of IDCODE.

2.4.1.3 Offset 03h: PRELOAD - PRELOAD for Boundary Scan

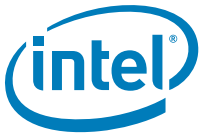
Bit	Type	Reset	Description
N	RW	0	**PRELOAD:** Command for Boundary Scan. Select the Boundary Scan register and put the boundary scan cell in functional mode. Used to load to the boundary scan cell with known input value shifting in from the TDI ping.

2.4.1.4 Offset 04h: CLAMP - CLAMP for Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**CLAMP:** Command for Boundary Scan. Clamp command drives the boundary scan value to the output pins but leaves the Bypass register as a selected register. It is the same as the EXTEST command except CLAMP selects the Bypass register.

2.4.1.5 Offset 08h: HIGHZ - HIGHZ for Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**HIGHZ:** Command for Boundary Scan. Put all output pins supporting the boundary scan in the High-Z state and leaves the Bypass register as a selected register. It is the same function as INTEST except the Bypass register is selected.



2.4.1.6 Offset 09h: EXTEST - EXTEST for Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**EXTEST:** Command for Boundary Scan. Select the Boundary Scan register and put the boundary scan cell in the output mode for DUT connectivity testing.

2.4.1.7 Offset 0Dh: EXTEST_TOGGLE - EXTEST TOGGLE Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**EXTEST_TOGGLE:** Special Command for Boundary Scan. The Extest toggle command toggles the boundary scan value to the output pins if the value in the boundary scan cell is 1, and drives constant 0 if the value in the boundary scan cell is 0. **Exception:** For USB2 and OPI pins: a value of 0 in the boundary scab cell will enable extest toggle, whereas the value of 1 will drive the constant output on to the pins.

2.4.1.8 Offset 0Eh: EXTEST_PULSE - EXTEST PULSE Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**EXTEST_PULSE:** Command for Boundary Scan 1149.6. The Extest pulse command generated a pulse at the output pins. The non 1149.6 pin behaves like the EXTEST command.

2.4.1.9 Offset 0Fh: EXTEST_TRAIN - EXTEST TRAIN Boundary Scan

Bit	Type	Reset	Description
N	RW	0	**EXTEST_TRAIN:** Command for Boundary Scan 1149.6 only. The Extest train command toggles the output pins. The non 1149.6 pin behaves like the EXTEST command.

2.4.1.10 Offset FFh: BYPASS - JTAG Bypass Register

Bit	Type	Reset	Description
N	RW	0	**BYPASS:** Select JTAG Bypass register. Connect the TDI to the TDO by a flop. The TDO value follows TDI after 1 TCK clock during the data register shift. The data register capture this register returns value of 0.

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